

Implementation of All 27 Possible Univariate Ternary Logics With a Single ZnO Memristor

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Abstract—Memristors with small size, fast speed, low power, CMOS compatibility and nonvolatile modulation of device resistance are promising candidates for the next-generation data storage and in-memory logic computing paradigm. In comparison to the binary logics enabled by memristor devices, multi-valued logics can provide higher computation efficiency with simple operation scheme, reduced circuit complexity, and smaller chip area. In this contribution, we demonstrate that all the 27 univariate ternary logic operations can be realized with a single ZnO three-state resistive switching memristor in at most three steps. The nonvolatile modulation characteristics of the memristor allow the read step to be independent of the logic operation and capacitate logic-in-memory applications. The present methodology could be beneficial for constructing future high-performance computation architectures.

Index Terms—Memristor, multi-state switching, nonvolatile, ternary logic.

I. INTRODUCTION

THE exponential increase in current digital communication for market trend analysis, real-time image processing, machine-learning and etc., arises great demand for powerful computation capability with enormous storage capacity and superior processing efficiency. However, Moore's Law that dominates the miniaturization campaign of the semiconductor industry over the past 60 years is approaching

its foreseeable end, as the electronic devices shrinking to a few nanometer encounter serious problems of current leaking, heat generation, and tremendous fabrication costs [3]. The frequent data shuttling between the separated memories and processors of the von Neumann architecture also leads to high power and speed costs that deteriorate the system's overall performance [4]. Therefore, novel electronic devices and new computation paradigm that can extend the lifetime of Moore's Law and overcome the von Neumann communication bottleneck are highly desired in the big data and artificial intelligence (AI) era [5], [6].

Resistive switching memristors [7], theoretically proposed by Chua [1] and first physically demonstrated by HP laboratory in 2008 [2], are considered as promising candidates for the next-generation data storage technique with their simple structure, small size, fast speed, low power consumption, and compatibility with the CMOS platform [8]–[10]. The nonvolatile modulation of device resistance also enables in-memory computation, wherein the logic output can be stored *in situ* in the same memory unit [11]–[14]. In recent years, various memristive logic concepts, including the Material Implication Memristor Logic (IMPLY), Memristor-Ratioed Logic (MRL), Memristor Aided Logic (MAGIC), CMOS/Memristor Threshold Logic, CMOS-like Memristor Complementary Logic, Parallel Input-Processing Memristor Logic and etc., [15]–[19], have been implemented to complete all the 16 Boolean logic operations. In comparison to the state-of-the-art binary scheme, multi-valued logic (MVL) is expected to perform more efficient in-memory computing task, as an increase in the amount of data that each word or bitline can carry may reduce the total numbers of wire connection and save the effective chip area [20]. It also provides a more effective solution to complex and cumbersome problems in binary logic gates. For instance, establishing a three-branch circuit or even multiplexer with higher-order logics can avoid substantial embedding of two-branch circuits and simplify the flowchart of program design. This is of significant importance for pattern recognition and expert system in the field of AI [21], [22]. Compared with traditional CMOS logic circuits, memristor-based logic circuits can achieve polymorphic storage and operation, which greatly reduces the number of devices and achieves lower power consumption and faster speed.

The total number of bivariate functions $(f(x, y) \in \{0, 1, 2\})$ in ternary logic is 19683, whereas there are only 16 $(f(x, y) \in \{0, 1\})$ in binary logic. It is difficult to screen

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TABLE I
ALL TERNARY UNIVARIATE FUNCTION

x	f_0	f_1	f_2	f_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}	f_{11}	f_{12}	f_{13}	f_{14}	f_{15}	f_{16}	f_{17}	f_{18}	f_{19}	f_{20}	f_{21}	f_{22}	f_{23}	f_{24}	f_{25}	f_{26}
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	2	2
1	0	0	0	1	1	1	2	2	2	0	0	0	1	1	1	2	2	2	0	0	0	1	1	1	2	2	2
2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2	0	1	2

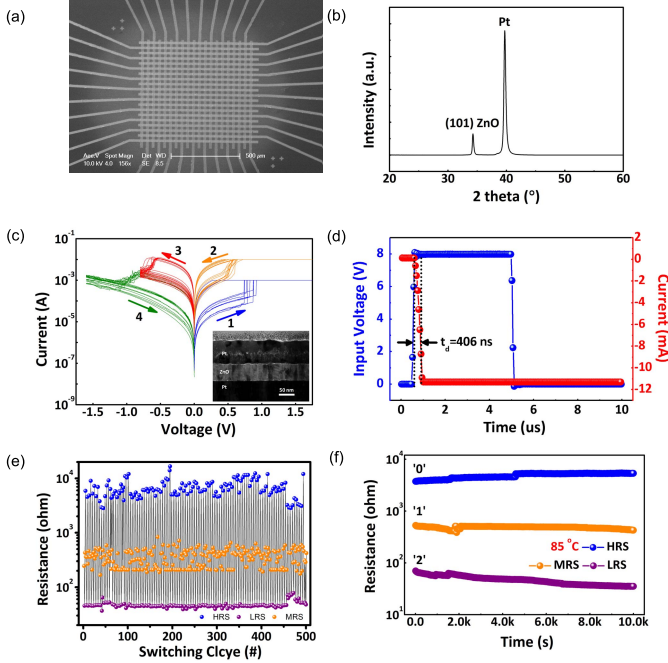


Fig. 1. (a) Scanning electron microscopic (SEM) image of the 20×20 Pt/ZnO/Pt memristor array. (b) X-ray diffraction pattern of the Pt/ZnO/Pt device. (c) Current-voltage characteristics of the memristor showing three-state switching behavior. Inset shows cross-sectional TEM image of the Pt/ZnO/Pt device sandwich structure. (d) Delay time between the input voltage pulse and the output current signals of the device. (e) Room-temperature endurance. (f) 85°C retention performance of the device.

out the basic operations that make up a complete set of operations from such a large number of functions. Considering that a simple complete set of Univariate function (NOT), AND, OR, binary operators is sufficient to construct any possible Boolean logic calculations; similarly, a three-valued univariate function complete set plus AND and OR operation can form a three-valued logical complete set. In this article, with the use of a single zinc oxide-based three-state memristor, we demonstrate the implementation of all 27 possible ternary logics with univariate operation in no more than three steps of initializing and writing. It provides all the possibilities for obtaining univariate basic operations in a three-valued logic function. Our ternary logic scheme with a single memristor device may provide an efficient approach for verification interacting and synthesis (VIS), future MVL circuit design and so on.

II. EXPERIMENTS

The ZnO-based resistive switching memristors were fabricated by photolithography and RF magnetron sputtering deposition into a 20×20 crossbar array [Fig. 1(a)].

Bottom electrode (BE) strips with the width of $20\ \mu\text{m}$ and the length of 10 mm were defined with a positive photoresist under UV lithography and deposited with Pt by sputtering on commercial Si substrate. ZnO was then sputtered at room temperature in pure Ar atmosphere, followed by lithographical deposition of top electrode (TE) strips with the width of $20\ \mu\text{m}$ and length of 10 mm. The thicknesses of each layer of the Pt/ZnO/Pt devices are measured as 70, 50, and 150 nm, respectively. X-ray diffractive pattern confirms the presence of (101) ZnO in the as-fabricated device.

The top and bottom electrodes of the memristor devices are defined as terminal T_1 and T_2 , respectively. The electrical measurements were performed on an Agilent B1500A semiconductor parameter analyzer equipped with a B1530A fast measurement unit. During the set operation in pulse mode, the device can be programmed from the initial high resistance state (HRS) to mediate resistance state (MRS) with a compliance current (CC) preset of 1 mA. Increasing the CC preset to 10 mA will further switch the device from MRS to the low resistance state (LRS).

III. RESULT AND DISCUSSION

The development of multiple-valued logic began in 1921 with the study of Post [23]. Table I lists all the 27 ternary univariate function ($f(x) \in \{0,1,2\}$) that can be categorized into several groups. With the aid of the AND and OR operations, certain groups of the univariate functions can be used to form a three-valued functional complete set. For instance, Rohleder selected f_{21} , f_2 , and f_8 as the basic operations [24] in 1954, while later Goto chose f_{21} , f_{18} , f_6 , and f_2 as alternative candidates [25]. In 1958, Muholdorf affirmed Goto's scheme and demonstrated that the selection of f_{18} , f_6 , and f_2 (known as j operations, literal operations, or threshold operations) is sufficient to be functional complete without f_{21} [26].

Resembling the evolution trend from triode, transistor to CMOS for designing traditional very large scale integration (VLSI) binary logic circuits, progress in multiple-valued logic (MVL) depends much on the development of devices that are inherently suitable for MVL operation. The device needs to have multi-resistance stability, low operating voltage, high-temperature tolerance, etc. and is better to be compatible with the CMOS platform. Resistive switching memristors with multi-level conductance states are promising candidates when considering these requirements.

Generally, memristor operates with the filamentary conduction mechanism, wherein the formation, annihilation,

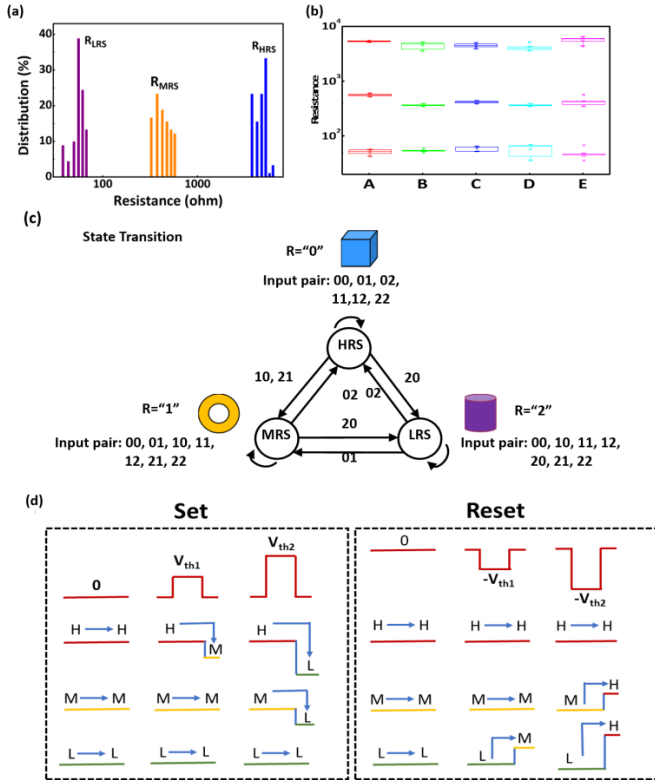


Fig. 2. (a) Distribution of the HRS, MRS, and LRS resistances of the Pt/ZnO/Pt memristor device retraced from ~ 100 switching cycles. (b) Box chart of five devices in HRS, MRS, and LRS resistance states. (c) Transition diagram of the memristor device between the three resistance states. (d) Resistance state transitions between the three resistance states at different pulse voltages.

and regeneration of the conductive filaments (CFs) via ion migration and solid-state redox reaction can modulate the device resistance/conductance significantly [27]. Noting that the mobile ions usually migrate along the point defects and grain boundaries, oxide thin films with cut-through microstructure are favorable for the formation of straight filaments and their confined evolution, which can lower the switching variation caused by the stochastic disruption and reformation of the otherwise branched CFs. With these concerns, we fabricated zinc oxide thin film with the columnar structure on Pt strip coated silicon substrates as the switching layer to construct memristor devices and 20×20 crossbar array [Fig. 1(a)]. X-ray diffractive pattern clearly confirms the presence of (101) ZnO in the as-fabricated device [Fig. 1(b)] while the thicknesses of each layer of the Pt/ZnO/Pt devices are measured as 70, 50, and 150 nm, respectively, through transmission electron microscopic (TEM) observation [Insert of Fig. 1(c)]. Upon programming the Pt/ZnO/Pt structure with a forming voltage of 7.8 V, the current-voltage characteristic of the device in dc sweeping mode shows obvious bipolar resistive switching behavior and a large memory window suitable for multi-level modulation [Fig. 1(c)]. By varying the CCs and RESET-stop voltages, the device can be cyclically switched between HRS, MRS, and LRS, respectively. When being swept positively with a CC preset of 1 mA, the device can be programmed from the initial HRS to MRS at the voltage of ~ 0.8 V in Sweep 1. Increasing the CC preset to

TABLE II
 TRUTH TABLE FOR 17 TWO-STEP TERNARY LOGICS

Logic Function	Initial State	Writing		Logic Output
		T ₁	T ₂	
F_0	0	0	$q(0, 1, 2)$	0, 0, 0
F_1	0	$q(0, 1, 2)$	V_1	0, 0, 1
F_2	0	$q(0, 1, 2)$	V_{base}	0, 0, 2
F_5	0	$q(0, 1, 2)$	0	0, 1, 2
F_9	0	V_{th1}	$q(0, 1, 2)$	1, 0, 0
F_{18}	0	V_{th2}	$q(0, 1, 2)$	2, 0, 0
F_4	1	$q(0, 1, 2)$	V_2	0, 1, 1
F_{12}	1	0	$q(0, 1, 2)$	1, 1, 0
F_{13}	1	$q(0, 1, 2)$	V_1	1, 1, 1
F_{14}	1	$q(0, 1, 2)$	0	1, 1, 2
F_{22}	1	V_2	$q(0, 1, 2)$	2, 1, 1
F_{21}	2	0	$q(0, 1, 2)$	2, 1, 0
F_8	2	$q(0, 1, 2)$	V_{th2}	0, 2, 2
F_{17}	2	$q(0, 1, 2)$	V_1	1, 2, 2
F_{24}	2	V_{base}	$q(0, 1, 2)$	2, 2, 0
F_{25}	2	V_1	$q(0, 1, 2)$	2, 2, 1
F_{26}	2	$q(0, 1, 2)$	0	2, 2, 2

10 mA will further switch the device from MRS to LRS at ~ 0.6 V in Sweep 2. Reversing the voltage polarity can switch the device from LRS to MRS and HRS in Sweeps 3 and 4 sequentially, wherein the stopping voltages of -0.8 and -1.6 V are used accordingly. The three-state switching can also be achieved with pulse mode operation, wherein the threshold voltages of 0.7 V (V_{th1}), 1.4 V (V_{th2}), -0.7 V ($-V_{th1}$) and -1.4 V ($-V_{th2}$) can switch the device between HRS, MRS and LRS, respectively. The switching can occur within ~ 400 ns [Fig. 1(d)], showing potentially fast speed for practical applications. The device shows good endurance characteristics in ~ 500 resistive switching cycles [Fig. 1(e)], and all the resistance states can be maintained at 25 °C for at least 10^4 s, and also have good retention at 85 °C [Fig. 1(f)].

Cumulative histogram of ~ 100 switching traces reveals that the HRS, MRS, and LRS resistances are well distinguished within different ranges [Fig. 2(a)], viz. 3.5–6.5 k Ω , 300–600 Ω , and 30–70 Ω . We also tested the cycling characteristics of many of the devices in the array (each device cycled 100 times) and randomly selected five sets of drawn box chart [Fig. 2(b)], and experimental results show that the HRS, MRS, and LRS resistances are well-differentiated in different ranges. These resistances are defined as the initial logic state or logic output state of the memristor as “0,” “1,” and “2,” respectively. The pulse voltages applied onto either T₁ or T₂ terminal serve as the univariate input signals. Zero voltage (0 V) represents logic “0,” $V_1 = 0.8$ V stands for

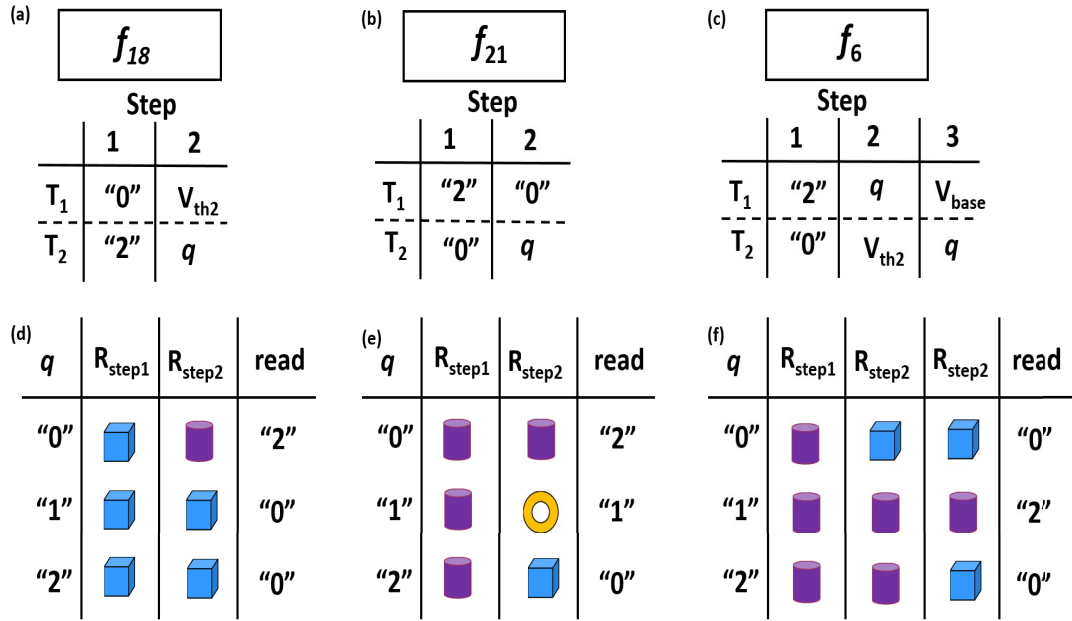


Fig. 3. Theoretical scheme of the two-step operation for the logic functions (a) and (d) F_{18} , (b) and (e) F_{21} , and (c) and (f) three-step operation for logic function F_6 .

logic “1” while $V_2 = 1.6$ V is taken as logic “2.” According to the state transition diagram shown in Fig. 2(c), different combinations of the input signals can program the memristor between three logic states, allowing the implementation of ternary logics. The first and second digits of the input pair shown in Fig. 2(c) represent the voltages applied onto the top and BEs of the memristor, respectively. For instance, the input pair “10” means $T_1 = “1”$ and $T_2 = “0.”$ The changing of the HRS, MRS, and LRS resistances after the application of the pulse operation is schematically shown in Fig. 2(d). “L,” “M,” “H” means “LRS,” “MRS,” and “HRS,” respectively. As an example, with the input of 0.8 V (“1”) during the SET process, the device resistance can only be programmed into MRS if the initial state is HRS. Otherwise, the device resistance state will remain unchanged.

Based on the above definitions, 27 ternary logics can be realized within no more than three sequential steps of initializing and writing(s), wherein the initialization step can program the memristor to a required state by applying an appropriate voltage pulse to the device. As summarized in Table II, upon fixing the initial logic state of the device and one of the terminal voltage inputs, one more step univariate writing to the other terminal can implement 17 ternary logics. Herein, the variable q takes the values “0,” “1” or “2,” and V_{base} is defined as 0.2 V. The change in the device resistance depends on $V_{T1}-V_{T2}$. The output logic (final resistance) state of the memristor is stored directly in the same device and can be readout by an additional independent read step with a small voltage pulse. Note that the implementation of the logic functions in the tables is not unique. For instance, logic F_5 can be also be implemented as ($T_1 = q$, $T_2 = V_2$) with the initial logic state of “2” for the memristor.

The remaining ten ternary logic functions can be realized by a three-step scheme, wherein the ZnO memristor is written

TABLE III
TRUTH TABLE FOR 10 THREE-STEP TERNARY LOGICS

Logic Function	Initial State	Writing		Writing		Logic Output
		T_1	T_2	T_1	T_2	
F_3	0	q	0	0	q	0, 1, 0
F_{10}	0	V_{th1}	q	q	V_1	1, 0, 1
F_{11}	0	V_{th1}	q	q	V_{base}	1, 0, 2
F_{19}	0	q	V_1	V_{th2}	q	2, 0, 1
F_{20}	0	V_{th2}	q	q	V_{base}	2, 0, 2
F_{23}	0	V_{th2}	q	q	0	2, 1, 2
F_6	2	q	V_{th2}	V_{base}	q	0, 2, 0
F_7	2	V_1	q	q	V_{th2}	0, 2, 1
F_{15}	2	q	V_1	V_{base}	q	1, 2, 0
F_{16}	2	q	V_1	V_1	q	1, 2, 1

twice after the initialization operation. In the first writing step, one of the terminals (e.g., T_2 in F_3 logic function) voltage input is fixed, and the univariate q writing operation to the other terminal (T_1 , accordingly). In the second writing step, the fixed and varying terminals interchange with one another, as summarized in Table III. The logic outputs in each function correspond to the input variable q of “0,” “1,” and “2,” respectively.

Fig. 3 shows a theoretical operation scheme of the f_{18} , f_{21} , and f_6 functions. Step one is always the initialization process, while steps two and third are the writing processes. R_{step1} , R_{step2} , and R_{step3} are device resistance states read by a small voltage, after the initialization and writing operations, respectively. For the implementation of logic F_6 [Fig. 3(c) and (f)], the ZnO memristor is first programmed to logic “2.” Then, T_2 is fixed as V_{th2} [Fig. 3(c)] and input pulse voltages

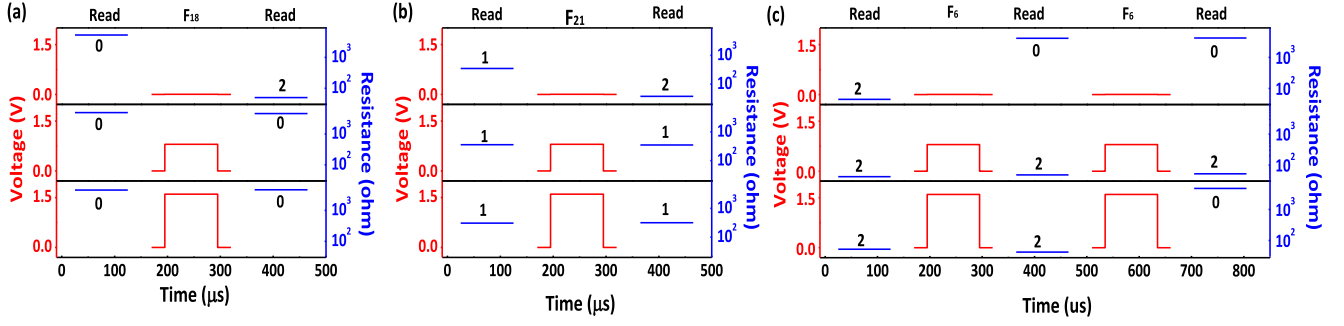


Fig. 4. Experimental results of the two-step operations for the logic functions (a) F_{18} and (b) F_{21} and (c) Three-step operation for logic function F_6 .

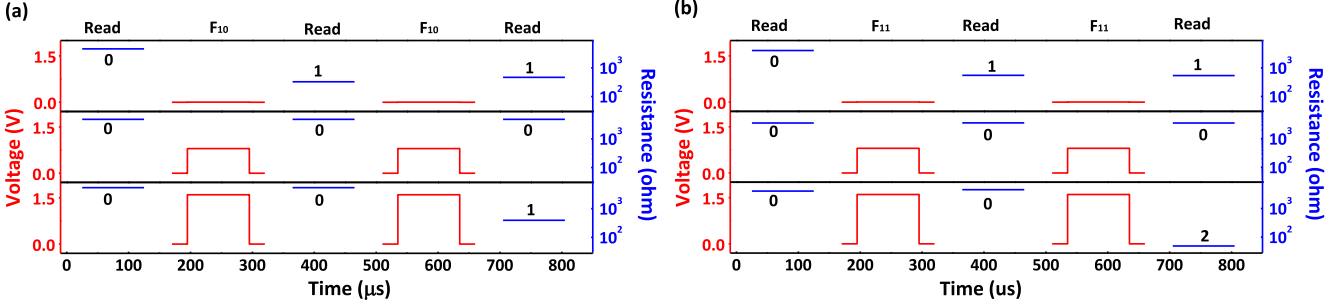


Fig. 5. Experimental results of the three-step operations for the logic functions (a) F_{10} and (b) F_{11} .

(0, 0.8, and 1.6 V) are applied onto T_1 , respectively. Afterward, T_1 is fixed as V_{base} , while input pulse voltages (0, 0.8, and 1.6 V) are applied onto T_2 . An additional readout step is finally employed to verify the achieved logic output and function. Logic operations of f_{18} and f_{21} can be performed similarly [Fig. 3(a) and (d) and (b) and (e)].

As a proof-of-concept, we demonstrate the experimental implementation of the two-step ternary logics, F_{18} and F_{21} , and the three-step ternary logic F_6 , as shown in Fig. 4. The blue line represents the initial resistance or output resistance logic states of the device while the red line stands for the voltage pulse input variables. For logic F_{18} , the ZnO memristor is initially programmed to logic “0” with the resistance of 3.7–4.4 k Ω and the T_1 terminal is fixed as $V_{\text{th}2}$ [Fig. 4(a)]. When the voltage pulse with the amplitude of 0 V (logic “0”), 0.8 V (logic “1”), and 1.6 V (logic “2”) are applied onto the T_2 terminal, respectively, the final resistance of the device are recorded as 50 Ω (logic output “2”), 3.7 k Ω (logic output “0”), and 3.8 k Ω (logic output “0”). Consistent with that summarized in Table II, logic function F_{18} is thus achieved with the two-step operation ($\text{Initial} = \text{“0”}$, $T_1 = V_{\text{th}2}$, $T_2 = q$). Logic F_{21} can be realized similarly, by fixing the initial logic state of the memristor as “2” and applying writing voltage variables q to T_2 [Fig. 4(b)].

According to Table III, the three-step operation of logic F_6 can be achieved, by fixing the memristor initial state to logic “2” and applying variables q to T_1 and T_2 , sequentially [Fig. 4(c)]. Note that the implementation of the logic functions in the tables is not unique. For instance, logic F_6 can also be implemented as $T_1 = V_{\text{base}}$, $T_2 = q$; $T_1 = q$, $T_2 = V_{\text{th}2}$ with initial logic state of “2” for the memristor. We show two similar but not the identical operation of logic function F_{10} and

F_{11} [Fig. 5] to indicate the operation window of the device. According to the experimental results in Figs. 4 and 5, we can clearly distinguish the output logic function values.

The scaling down of silicon devices reached the physical limits around the year 2000. Using 13.5-nm extreme UV lithography, the scaling trend is expected to result in the achievement of 5 and 3.5-nm technology nodes by 2025. After the year 2025, semiconductor electronics will likely to enter in a hyperscaling era, resistive random access memory (RRAM) devices process information more efficiently without further physical scaling. One approach is to increase the information density of the logic operation unit or interconnect lines using multi-state logic. Comparing with a binary logic system, the ternary logic system can theoretically reduce the device count and interconnect lines by 37% and 36%, respectively. Furthermore, it has the advantages of good reversibility, low power consumption, and near-linear analog switching. Our results show the read step to be independent of the logic operation and capacitate logic-in-memory by the use of ZnO-based three-state memristor. We anticipate ZnO-based three-state memristor would shed light on future applications on high-performance computation architectures.

IV. CONCLUSION

In conclusion, we produced a bipolar three-state resistive switching memristor device with zinc oxide as the switching layer and proposed an approach to implement ternary logics. Through univariate operation in no more than three steps of initializing and writing(s), all the 27 possible ternary logics can be realized with a single memristor cell. Univariate basic operations, and combined with AND, OR operations can form a three-valued complete set of operations. In addition to the

intrinsic storage capability of the memristor for in-memory computing with logic operations, the higher-order computation scheme with the present ternary routes may further enhance the efficiency of neuromorphic computing with reduced wire connections and fewer chip areas. Future study on cascading in larger logic circuits should be conducted for the realization of more complex logic and computing functions.

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