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Improving Unipolar Resistive Switching Uniformity with Cone-Shaped Conducting Filaments and Its Logic-In-Memory Application

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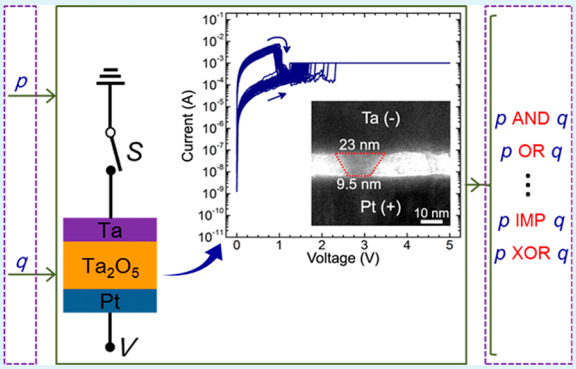
Supporting Information

ABSTRACT: Resistive random access memory (RRAM) with inherent logic-in-memory capability exhibits great potential to construct beyond von-Neumann computers. Particularly, unipolar RRAM is more promising because its single polarity operation enables large-scale crossbar logic-in-memory circuits with the highest integration density and simpler peripheral control circuits. However, unipolar RRAM usually exhibits poor switching uniformity because of random activation of conducting filaments and consequently cannot meet the strict uniformity requirement for logic-in-memory application. In this contribution, a new methodology that constructs cone-shaped conducting filaments by using chemically a active metal cathode is proposed to improve unipolar switching uniformity. Such a peculiar metal cathode will react spontaneously with the oxide switching layer to form an interfacial layer, which together with the metal cathode itself can act as a load resistor to prevent the overgrowth of conducting filaments and thus make them more cone-like. In this way, the rupture of conducting filaments can be strictly limited to the tip region, making their residual parts favorable locations for subsequent filament growth and thus suppressing their random regeneration. As such, a novel "one switch + one unipolar RRAM cell" hybrid structure is capable to realize all 16 Boolean logic functions for large-scale logic-in-memory circuits.



KEYWORDS: *unipolar resistive switching, cone-shaped conducting filament, switching uniformity, logic-in-memory, Ta_2O_5*

1. INTRODUCTION

In today's big data era, the pursuit of better computing is unprecedentedly urgent, as digital information is generated in great diversity, high volume, and at exponentially growing speed.[1] One promising solution is to construct beyond von-Neumann computers using resistive random access memory (RRAM),[2−5] which features inherent logic-in-memory capability with high speed, high efficiency, and low power characteristics.[6−11] Basically, RRAM can be classified into unipolar[12−15] and bipolar[16−19] types. Despite being slightly inferior in endurance, power consumption, and variability than the bipolar one, unipolar RRAM has exclusive advantages for logic-in-memory application. First, its single polarity operation scheme allows two-terminal diodes as selectors to settle the sneak-path issue in crossbar arrays, thus guaranteeing the highest integration density of $4F^2$/cell (F: the minimum feature size).[9,10] Indeed, the RRAM test chip with a record storage capacity of 32 Gb was made with such an integration architecture by SanDisk and Toshiba.[20] Second, the single polarity operation scheme also enables simplified peripheral control elements to support large-scale integrated circuits.[21]

Great efforts have been devoted globally to realize beyond von-Neumann computation with unipolar RRAM. In 2011, Sun et al.[22] first realized the IMP function with two unipolar RRAM cells and one conventional resistor, following which Amrani et al.[23] proposed to perform the OR function using two unipolar RRAM cells and the NOT function using one unipolar RRAM cell and one conventional resistor. Very recently, Jang et al.[24] succeeded in implementing the NOR function based on three unipolar RRAM cells. All these logic functions are based on the voltage divider effect between the adopted circuit elements, which puts forward a strict requirement in the uniformity of switching parameters to guarantee reliable operations.[25] However, unipolar RRAM usually works on an intrinsic

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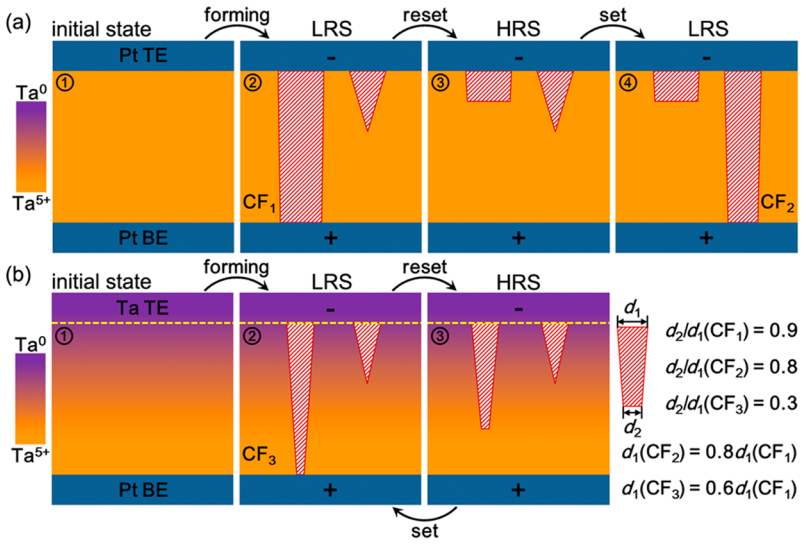

Figure 1. Schematic cathode material-dependent evolution processes of conducting filaments in unipolar RRAM cells. (a) In a unipolar Ta_2O_5 RRAM cell with a conventional inert Pt cathode. (b) In a unipolar Ta_2O_5 RRAM cell with a novel chemically active Ta cathode. The yellow dashed lines in (b) denote the nominal Ta TE/Ta_2O_5 interface. For simplicity, the switching mechanism with a single filament is assumed here.

filamentary switching mechanism and consequently exhibits poor switching uniformity because of the random activation of conducting filaments (CFs) at different locations.[12−15] To date, a number of methods including microstructure optimization,[26] doping with metal nanoparticles,[27−29] and electrode engineering[30,31] have been proposed to improve unipolar switching uniformity, wherein the principle strategy is to create favorable locations for the formation of CFs so as to suppress their random activation throughout the entire device. Nevertheless, the incompatibility of these methods with the standard CMOS technique makes them less practically applicable. The number of available logic functions achieved using unipolar RRAM is also limited to 4, given the fact that complete set of Boolean logic contains 16 operations. Therefore, simple yet effective approaches to improve the unipolar switching uniformity and to realize as many Boolean logic functions as possible with unipolar RRAM are still highly desired.

In this work, we propose and demonstrate a new methodology to improve the switching uniformity of unipolar RRAM by employing a chemically active metal cathode to construct cone-shaped CFs. Such a peculiar metal cathode will react spontaneously with the oxide switching layer to form an interfacial layer, which together with the metal cathode itself can act as a load resistor to prevent the overgrowth of CFs, thus making them more cone-like. Indeed, high-resolution transmission electron microscopy (TEM) observation suggests that cone-shaped metallic Ta CFs are formed in unipolar Ta_2O_5 RRAM cells with chemically active Ta cathodes, which are remarkably different from the normally observed cylindrical ones.[12,13,15] With their cone-shaped configuration, the rupture of these Ta CFs is strictly limited to the tip region, making their residual parts rather than the other partially formed Ta protrusions favorable locations for subsequent filament growth. Thus, the random activation of CFs is significantly hindered, and highly reduced switching nonuniformity with a minimum of 5.5% is resulted. On the basis of the superior electrical behavior of such cone-shaped CF devices, a "one switch + one unipolar RRAM cell" hybrid structure is constructed to perform logic functions. Theoretical analysis and experimental results reveal that 14 Boolean logic functions can be implemented in no more than three sequential logic cycles, whereas the remaining NOR and XNOR functions can be realized with additional algorithmic steps or with the aid of a conventional CMOS inverter in control circuits.

2. EXPERIMENTAL SECTION

2.1. Device Fabrication. Sample Ta/Ta_2O_5(∼10 nm)/Pt and reference Pt/Ta_2O_5(∼10 nm)/Pt unipolar RRAM cells were both fabricated on commercial Pt(∼120 nm)/Ti(∼15 nm)/SiO_2/Si substrates. First, the substrates were ultrasonically cleaned in sequence in acetone, ethanol, and deionized water (8 min for each solvent). Next, the Ta_2O_5 layer was deposited on them by radio-frequency magnetron sputtering with a ceramic Ta_2O_5 target at room temperature and in a pure argon atmosphere (∼0.4 Pa). Third, a photoresist layer was spin-coated on the Ta_2O_5 layers and then patterned with isolated holes (50 μm in diameter) by a conventional ultraviolet lithography process. Finally, a ∼60 nm Ta or Pt layer was deposited by direct current (dc) magnetron sputtering at room temperature and in a pure argon atmosphere (∼0.4 Pa), after which a lift-off process was conducted and ended with isolated Ta or Pt top electrodes (TEs).

2.2. Device Characterization. All electrical measurements were conducted using a semiconductor device analyzer (B1500A, Agilent) in an atmospheric environment and at room temperature. External voltages were always applied to the common Pt bottom electrode (BE), with the isolated Ta and Pt TEs grounded. To characterize the device microstructure and to observe CFs, cross-sectional specimens were cut from both pristine and programmed RRAM cells using a focused ion beam (FIB) system (Auriga, Carl Zeiss) and then examined using a high-resolution TEM (Tecnai F20, FEI Company) with energy-dispersive X-ray spectroscopy (EDS) and electron energy loss spectroscopy (EELS) analytical accessories.

3. RESULTS AND DISCUSSION

Unipolar RRAM cells usually have a metal/insulator/metal trilayer structure, with binary metal oxides (such as NiO,[26,28] ZnO,[12,15] TiO_2,[27,32] and Ta_2O_5[13,33,34]) as the switching layer and inert metals (typically Pt[12,26−28,32−34]) as both electrodes. Under external voltage stimuli, they can be reversibly switched between a high-resistance state (HRS) and a low-resistance state (LRS), and the switching from the HRS to LRS is denoted as a set process with its opposite as a reset process. In this work,

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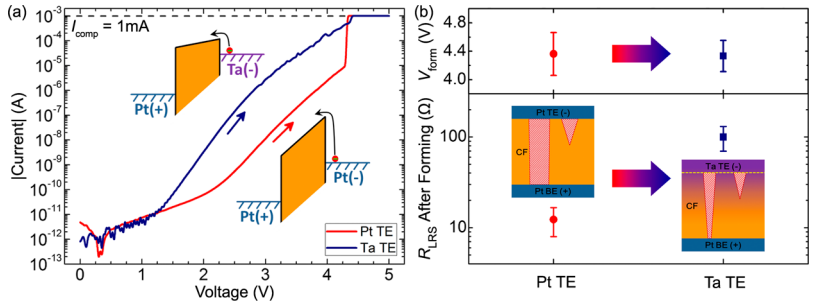

Figure 2. Comparative forming process analysis between reference Pt/Ta_2O_5(~10 nm)/Pt and sample Ta/Ta_2O_5(~10 nm)/Pt unipolar RRAM cells. (a) Representative forming processes of the reference Pt TE and the sample Ta TE RRAM cells. The insets show schematic band structures during the forming process. (b) Comparisons of V_{form} and R_{LRS} after forming between the reference Pt TE and sample Ta TE RRAM cells. For both types of RRAM devices, 10 cells were randomly chosen for such statistical analysis.

Ta_2O_5 is selected as the switching layer because it has been acknowledged as a model and promising binary metal oxide storage medium for RRAM.[34,35] Figure 1a shows the schematic evolution process of CFs in a unipolar Ta_2O_5 RRAM cell with Pt as both the TE and BE. Generally, the memory cell will have a uniform Ta_2O_5 switching layer, as well as clear Pt TE/Ta_2O_5 and Ta_2O_5/Pt BE interfaces (① in Figure 1a). Upon forming with the Pt BE positively biased with respect to the Pt TE, a complete CF denoted as CF_1 (② in Figure 1a) will grow from the cathode (Pt TE) to the anode (Pt BE) and then short-circuit the electrode pair.[13,33,35−37] Other partially formed CFs may also exist in the Ta_2O_5 switching layer.[14,32] According to the previous in situ TEM observation and theoretical analysis,[12,13,15,33] CF_1 will be cylinder-like in the symmetric device structure. That is, if d_1 and d_2 represent the diameters of a CF at its wider and narrower ends, respectively, the d_2/d_1 of CF_1 will be close to 1. Thermal simulation by Chang et al.[38] suggests that the high temperature region caused by the Joule-heating effect can cover the most part of cylindrical CF_1. The reset process of unipolar RRAM cells is caused mainly by thermal dissolution of existing filaments.[7−9] Hence, most part of CF_1 may be disrupted in the subsequent reset process, making the residual part even shorter than the partially formed CF (② → ③ in Figure 1a). If so, another CF, denoted as CF_2, will be naturally activated in the following set process (③ → ④ in Figure 1a), resulting in the random evolution of CFs at different locations. Because CF_1 and CF_2 are relatively different in size and shape, large fluctuation in switching parameters including the resistance values of the LRS and HRS (R_{LRS} and R_{HRS}) and the threshold voltages of set and reset processes (V_{set} and V_{reset}) will be demonstrated.[8,9,14]

To improve the switching uniformity, we herein propose a new simple methodology of constructing cone-shaped CFs in unipolar RRAM cells, by replacing the conventional inert Pt cathode with the chemically active Ta cathode (① in Figure 1b). The key is to take advantage of the spontaneous redox reaction at the Ta/Ta_2O_5 interface (precisely, the out-diffusion of oxygen ions from Ta_2O_5 into Ta) to generate an interfacial layer containing a large amount of oxygen vacancies and/or tantalum suboxides.[39,40] This interfacial layer will act as a load resistor and thus prevent the overgrowth of CFs during forming and set processes through the voltage divider effect.[41,42] Also, the Ta electrode itself with a higher resistivity than the Pt electrode can contribute to such a voltage divider effect. Kim et al. have demonstrated the growth of CFs from the cathode to the anode[36,37] and, more importantly, the gradual evolution of CFs' shape from conical to cylindrical as their overall size increases.[7,43] Therefore, because of the prevention of overgrowth by the interfacial layer and the Ta electrode itself, a more cone-like CF denoted as CF_3 (② in Figure 1b) is expected to grow from the Ta TE to the Pt BE and then short-circuit the electrode pair in Ta/Ta_2O_5/Pt RRAM cells during forming with the Pt BE positively biased with respect to the Ta TE. Thermal simulation by Menzel et al.[44] indicates that the high temperature region caused by the Joule-heating effect locates only at the tip region of conical CF_3. In this case, during the subsequent Joule-heating-dominated reset process, the rupture of conical CF_3 can be constrained strictly at its tip region (② → ③ in Figure 1b), differing significantly from the case of cylindrical CF_1 whose most part is disrupted (② → ③ in Figure 1a). As such, the residual part of ruptured CF_3 will be much longer than other partially formed CFs, resulting in the preferential occurrence of the recovery of CF_3, rather than the activation of a completely new CF, in the following set process (③ → ② in Figure 1b). Because the random activation of CFs at different locations is suppressed, a highly uniform unipolar resistive switching behavior can be expected in Ta/Ta_2O_5/Pt RRAM cells.[30,31] It is worth mentioning herein that previous works on Ta/Ta_2O_5/Pt RRAM are all focused on bipolar resistive switching with a Ta TE as th eanode,[39−41] which are remarkably different from the current work on unipolar resistive switching with a Ta TE as the cathode.

To confirm our proposal, both Ta/Ta_2O_5(~10 nm)/Pt and reference Pt/Ta_2O_5(~10 nm)/Pt unipolar RRAM cells (circular shape with 50 μm diameter) were fabricated and characterized first by high-resolution TEM with EDS analytical accessories (Figure S1, Supporting Information). The rather obscure Ta TE/Ta_2O_5 interface and the noticeable increase in oxygen distribution from 9.9 nm in the reference Pt TE sample to 11.2 nm in the Ta TE sample can demonstrate the occurrence of spontaneous interfacial reaction between Ta TE and Ta_2O_5. Then, electrical measurements were conducted to investigate the switching behavior of Ta/Ta_2O_5(~10 nm)/Pt as well as reference Pt/Ta_2O_5(~10 nm)/Pt unipolar RRAM cells. Initially, both RRAM cells had an extremely high resistance of $\sim 10^{11}$ Ω because of their good insulating property of the sputtered Ta_2O_5 switching layer. To activate repeatable unipolar resistive switching, a forming process was necessary for both RRAM cells, during which a compliance current (I_{comp}) of 1 mA was adopted to prevent permanent breakdown, as shown in Figure 2a. The current level of the Ta TE RRAM cell after 1.5 V is obviously larger than that of the reference Pt TE RRAM cell, which is because of the easier injection of electrons from a Ta TE with a lower work function into the

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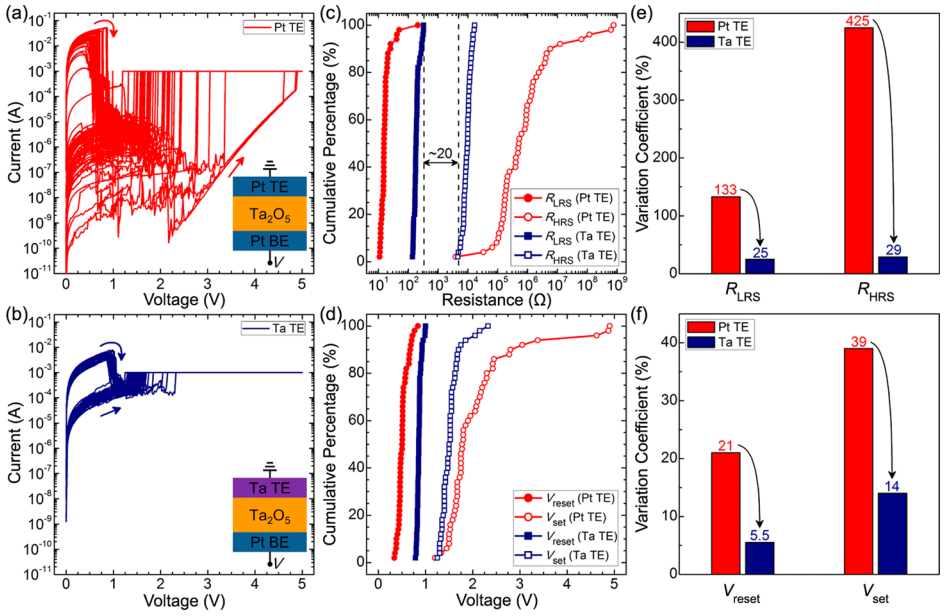

Figure 3. Comparative cycle-to-cycle switching uniformity analysis between reference Pt/Ta_2O_5(~10 nm)/Pt and sample Ta/Ta_2O_5(~10 nm)/Pt unipolar RRAM cells. *I*–*V* curves of 50 successive unipolar resistive switching cycles of a (a) representative reference Pt TE RRAM cell and of a (b) representative sample Ta TE RRAM cell. The insets in (a,b) show schematic device structures with measurement configuration. Cumulative distributions of (c) R_{LRS} and R_{HRS} and (d) V_{set} and V_{reset}. Variation coefficients of (e) R_{LRS} and R_{HRS} and (f) V_{set} and V_{reset}. The data in (c–f) were obtained based on the *I*–*V* curves in (a,b).

Table 1. Summary on μ and σ Values of the Switching Parameters R_{LRS}, R_{HRS}, V_{set}, and V_{reset}

	R_{LRS} (Ω)		R_{HRS} (Ω)		V_{set} (V)		V_{reset} (V)	
	Pt TE	Ta TE	Pt TE	Ta TE	Pt TE	Ta TE	Pt TE	Ta TE
μ	21.4	197.2	32.6 M	9.8k	2.10	1.53	0.52	0.87
σ	28.4	48.6	138.5 M	2.9k	0.82	0.21	0.11	0.048

Ta_2O_5 switching layer.[45] However, the two cells have an almost identical forming voltage (V_{form}) of ~4.4 V, which can be confirmed more solidly by the statistical result in the upper part of Figure 2b. This is readily understandable based on the consensus that, with the same positively biased electrode, V_{form} is determined mainly by the switching layer thickness.[46] The lower part of Figure 2b shows the comparison of R_{LRS} after forming between the reference Pt TE and sample Ta TE RRAM cells. One can easily see that the R_{LRS}, after forming of Ta TE RRAM cells (~100 Ω), is much larger than that of reference Pt TE RRAM cells (~10 Ω), which coincides well with our proposal in Figure 1 that thinner filaments will form in Ta TE RRAM cells because of the voltage divider effect caused by the interfacial layer and the Ta TE itself.

Comparative analyses of both cycle-to-cycle and device-to-device switching uniformity have been made between Ta/Ta_2O_5(~10 nm)/Pt and reference Pt/Ta_2O_5(~10 nm)/Pt unipolar RRAM cells. Figure 3a shows the current–voltage (*I*–*V*) curves of 50 successive unipolar resistive switching cycles of a representative reference Pt TE RRAM cell. As expected, poor cycle-to-cycle switching uniformity is observed because of the random activation of CFs in the entire device. In sharp contrast, Ta TE RRAM cells exhibit a highly uniform unipolar resistive switching behavior, as shown in Figure 3b. Such improvement in cycle-to-cycle switching uniformity can be revealed more clearly by the cumulative distributions of R_{LRS} and R_{HRS} in Figure 3c and of V_{set} and V_{reset} in Figure 3d, and also by the variations of R_{LRS}, R_{HRS}, V_{set}, and V_{reset} with a switching cycle number in Figure S3, Supporting Information. To provide a quantitative comparison, the variation coefficients of all switching parameters have been calculated by σ/μ (σ: standard deviation; μ: mean value). The detailed μ and σ values of each switching parameter are listed in Table 1. Figure 3e,f shows the variation coefficients of R_{LRS} and R_{HRS} and of V_{set} and V_{reset}, respectively. It is obvious that all coefficients of variation have been remarkably suppressed in Ta TE RRAM cells. In particular, the variation coefficient of R_{HRS} has been reduced to only ~7% of its reference value in Pt TE RRAM cells. For comparative analysis of device-to-device switching uniformity, 10 Ta TE RRAM cells as well as 10 reference Pt TE RRAM cells were randomly chosen, and 50 successive unipolar resistive switching cycles were measured for each cell. The obtained data were statistically analyzed and are provided in Figure S4, Supporting Information. Much better device-to-device switching uniformity has also been observed in Ta TE RRAM cells. These results unambiguously demonstrate the feasibility of improving unipolar switching uniformity by replacing the conventional inert Pt cathode with a chemically active Ta cathode. It is noteworthy that the improved unipolar switching uniformity by such a simple method in this work is found to be comparable or even better than that achieved by complex methods documented in the literature (Figure S5, Supporting Information),[26−31] which indicates a highly cost-effective performance of our method. In addition, the Ta TE RRAM cells evaluated in the dc voltage sweeping mode also exhibit much better unipolar switching endurance (>900 cycles) than reference Pt TE ones and good retention performance (Figure S6, Supporting Information). The endurance of Ta TE RRAM

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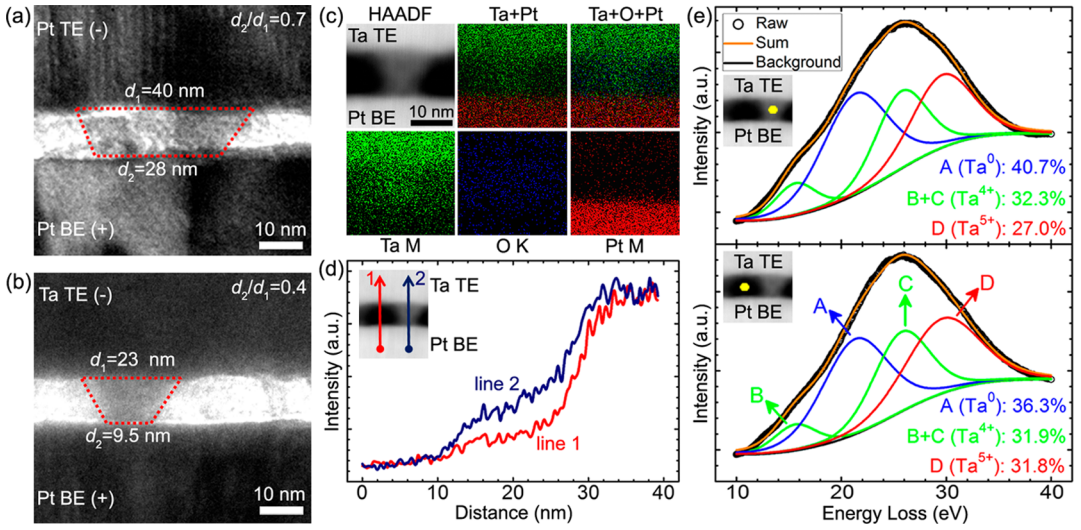
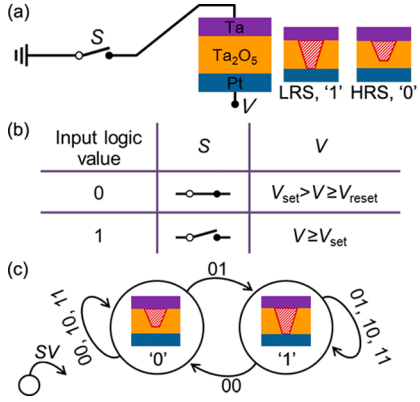


Figure 4. Direct TEM analysis on the conducting filaments in reference Pt/Ta_2O_5(~10 nm)/Pt and sample Ta/Ta_2O_5(~10 nm)/Pt unipolar RRAM cells. TEM images of representative CFs in (a) reference Pt TE and (b) sample Ta TE RRAM cells. (c) EDS mapping, (d) EDS line scan, and (e) low-energy EELS analysis around the CF in (b). The high-angle annular dark field scanning TEM images in (c–e) are used to denote the exact regions for each analysis. In (e), the raw data are fitted by referring to ref 46 and the area percentages of Ta^0, Ta^{4+}, and Ta^{5+}signals are provided.



(d)

Logic function	W1		W2		W3	
	S	*V*	*S*	*V*	*S*	*V*
True	0	1	-	-	-	-
False	0	0	-	-	-	-
p	0	*p*	-	-	-	-
q	0	*q*	-	-	-	-
NOT *p*	0	0	*p*	1	-	-
NOT *q*	0	0	*q*	1	-	-
p AND *q*	0	*p*	*q*	0	-	-
p NAND *q*	0	0	*p*	1	*q*	1
p OR *q*	0	1	*p*	*q*	-	-
p IMP *q*	0	*q*	*p*	1	-	-
p NIMP *q*	0	0	*q*	*p*	-	-
p RIMP *q*	0	*p*	*q*	1	-	-
p RNIMP *q*	0	0	*p*	*q*	-	-
p XOR *q*	0	0	*p*	*q*	*q*	*p*

Figure 5. The method for realizing 14 of 16 Boolean logic functions using a compact "one switch + one unipolar RRAM cell" hybrid structure. (a) Circuit sketch of the hybrid structure. (b) Correspondence between input logic values and physical signals of *S* and *V*. (c) Finite state machine of the Ta TE RRAM cell in (a). It depicts the state transition directions under each *SV* combination. (d) Detailed operation methods of 14 Boolean logic functions.

cells will certainly show further enhancement in pulse voltage mode for practical use in future, wherein the accumulation of serial voltage pulses in a single voltage sweeping operation that can lead to device aging is eliminated.

To further confirm the origin of switching uniformity enhancement in Ta TE RRAM cells, cross-sectional specimens of both types of RRAM cells were cut from LRS cells using an FIB system, and then the CFs therein were characterized by high-resolution TEM with EDS and EELS analytical accessories. To ensure that the captured CFs are the active ones for switching, cross-sectional specimens were deliberately cut from the close vicinity of contact points between the W-probe and the Pt or Ta TE because here is usually the active switching region.[47] Figure 4a shows the TEM image of a typical CF in the reference Pt TE specimen, which is indeed pseudo-cylindrical with a large d_2/d_1 of 0.7. In sharp contrast, cone-shape CFs with high conicity are found as expected in the Ta TE specimen, showing a much smaller d_2/d_1 of 0.4 in Figure 4b. Other similar CFs in each specimen were also captured and are shown in Figure S7, Supporting Information. These results indicate a switching mechanism with multiple filaments in our RRAM cells. Also, the overall size of CFs in the Ta TE specimen is obviously smaller than that in the reference Pt TE specimen, which verifies the effective role of the load resistor by the Ta/Ta_2O_5 interface as well as the Ta TE itself in preventing the overgrowth of CFs and also accords well with the larger R_{LRS} and V_{reset} of Ta TE RRAM cells in Figure 3c,d.[37] Meanwhile, the composition of CFs has been analyzed to better understand the switching mechanism, and the CFs in Ta TE RRAM cells were selected for such analysis because of their key role in this work. EDS mapping and the line scan results in Figure 4c,d clearly indicate a much higher Ta content within the CF region than that in the surrounding Ta_2O_5 layer. The O *K*-edge EELS result in Figure S8 (Supporting Information) also reveals a much lower O content within a CF region than that in its surrounding, suggesting that the formed CFs are oxygen-deficient in composition. To clarify the exact valance of Ta content within CFs, low-energy EELS spectra were obtained in both the CF region and the surrounding Ta_2O_5 layer and fitted accordingly (Figure 4e).[48] The Ta^0 content increases obviously from 36.3% in the surrounding Ta_2O_5 layer to 40.7% in the CF region, with the Ta^{5+} species decreasing from 31.8 to 27.0%

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accordingly, suggesting that the formation of cone-shaped metallic Ta CFs accounts for the improved unipolar switching uniformity in Ta TE RRAM cells. Besides, in good agreement with that observed in other Ta_2O_5 RRAM cells by the HP lab,[39] the formed Ta CFs are found to be amorphous based on fast Fourier transform (FFT) analysis (Figure S9, Supporting Information).

With such highly uniform unipolar switching in Ta TE RRAM cells with cone-shaped CFs, we have further explored their logic-in-memory application. The logic functions realized using unipolar RRAM to date are very limited in number, and each of them requires a unique circuit configuration, which is possibly because of the fact that only a single type of the input logic signal was used.[22−24] To overcome this problem, we herein propose a novel "one switch + one unipolar RRAM cell" hybrid structure, as schematically shown in Figure 5a. In this case, both the switch's physical state (S) and the external voltage (V) can be used as input logic signals. Herein, it is noteworthy that the switch is used to better understand and easily demonstrate the proposed novel logic concept in this work, whose function can be readily implemented by a popular transistor in practical use (Figure S10, Supporting Information). As for the output logic value after a certain logic operation, it is still automatically stored in the unipolar RRAM cell, whose nonvolatile HRS and LRS are defined as output "0" and "1", respectively.[22−24] Figure 5b shows the defined correspondence between input logic values and physical signals. That is, for S, input logic 0 and 1 mean that the switch is turned on and off, respectively, whereas for V, input logic 0 and 1 mean that it can write the Ta TE RRAM cell into state "0" and "1", respectively. With such a definition, the switching direction of the Ta TE RRAM cell under each SV combination can be found in Figure 5c. In detail, if initially, in the "0" state, the 01 combination switches the Ta TE RRAM cell into the "1" state, the other three combinations (00, 10, and 11) cannot change its memory state. In contrast, if initially, in the "1" state, the 00 combination switches it into the "0" state, the other three combinations (01, 10, and 11) cannot change its memory state. These can be mathematically expressed by

$$Z = (S \text{ OR } V)\cdot Z_0 + (S \text{ RNIMP } V)\cdot(\text{NOT } Z_0) \quad (1)$$

where Z_0 and Z represent the Ta TE RRAM cell's state before and after inputting a certain SV combination, respectively. With this equation, 14 of 16 Boolean logic functions are found to be feasible in no more than three sequential write cycles (denoted in sequence as W1, W2, and W3), as shown in Figure 5d. "p" and "q" in this figure are used conventionally to represent the two input logic variables. For example, the AND function can be realized in two write cycles with $SV = 0p$ in W1 and $SV = q0$ in W2. In detail, the intermediate state Z' after $SV = 0p$ in W1 is

$$Z' = (0 \text{ OR } p)\cdot Z_0 + (0 \text{ RNIMP } p)\cdot(\text{NOT } Z_0) = p \quad (2)$$

and thus the final state Z after $SV = q0$ in W2 is

$$\begin{aligned} Z &= (q \text{ OR } 0)\cdot Z' + (q \text{ RNIMP } 0)\cdot(\text{NOT } Z') \\ &= (q \text{ OR } 0)\cdot p + (q \text{ RNIMP } 0)\cdot(\text{NOT } p) = p \text{ AND } q \end{aligned} \quad (3)$$

The feasibility of the proposed logic operation methods in Figure 5d has been experimentally demonstrated by the combination of Figure 6 and Table 2. To ensure consistency, the Ta TE RRAM cell was initialized into the "0" state before performing each logic function. Such an initialization step is not necessary in practical application because it relates only to the detailed switching process during W1 but will not affect the state after W1. During the entire performing process, input logic 0 and 1 for V corresponded to a sweep of 0 V → 1.2 V → 0 V without I_{comp} and a sweep of 0 V → 3 V → 0 V with I_{comp} of 1 mA, respectively. After performing each logic function, a read cycle (R) was used to check the output logic value that was automatically stored in the Ta TE RRAM cell. For simplicity, only the results for the AND function are taken as an example to provide a detailed description. In W1, 0 and p were input into S and V, respectively (Figure 5d), which led to the following two cases. First, with $p = 0$, the SV combination was actually 00, which resulted in the closing of the switch and the applying of a 0 V → 1.2 V → 0 V sweep without I_{comp} on the Ta TE RRAM cell. Because the Ta TE RRAM cell had already been initialized into the "0" state before W1, it would stay unchanged during W1. If so, in W2 with $SV = q0$, neither the 00 ($q = 0$) combination nor the 10 ($q = 1$) combination could change the Ta TE RRAM cell's state (Figure 5c), corresponding respectively to output = p AND q = 0 AND 0 = 0 (Figure 6b1) and output = p AND q = 0 AND 1 = 0 (Figure 6b3). Second, with $p = 1$, the SV combination was actually 01 in W1, which resulted in the closing of the switch and the applying of a 0 V → 3 V → 0 V sweep with I_{comp} of 1 mA on the Ta TE RRAM cell. Because the Ta TE RRAM cell

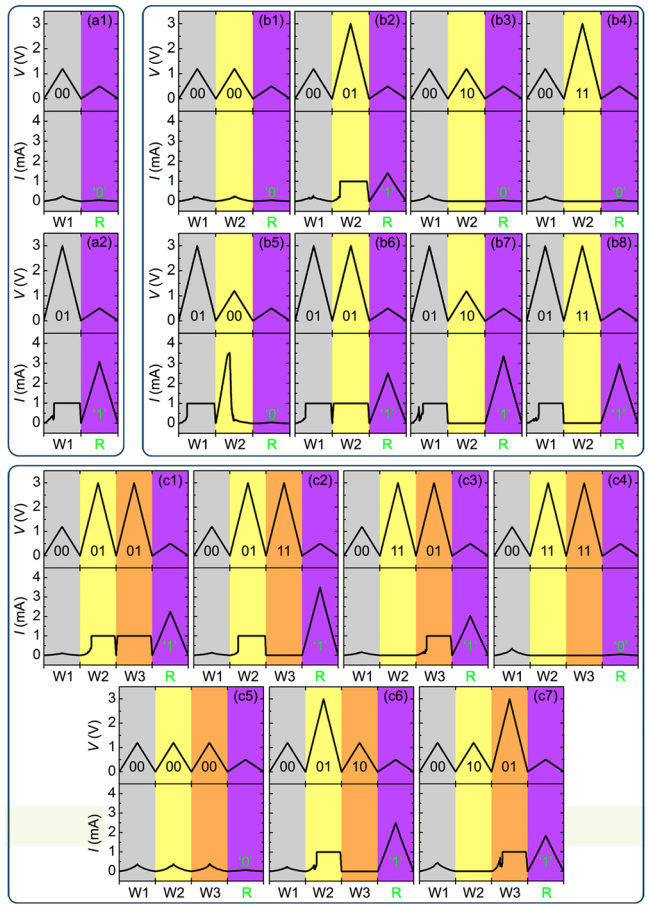

Figure 6. Experimental results of the 14 Boolean logic functions in Figure 5d. (a) Results of functions that can be completed using only one write cycle. (b) Results of functions that can be completed using two write cycles. (c) Results of functions that need to be completed using three write cycles. The periods of all write and read cycles are ~4 s.

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Table 2. Truth Table of the 14 Boolean Logic Functions in Figure 5d and Corresponding Experimental Results in Figure 6

	input		W1			W2			W3				
logic function	*p*	*q*	*S*	*V*	*SV*	*S*	*V*	*SV*	*S*	*V*	*SV*	output	experimental results
true	0	0	0	1	01							1	(a2)
	0	1	0	1	01							1	(a2)
	1	0	0	1	01							1	(a2)
	1	1	0	1	01							1	(a2)
false	0	0	0	0	00							0	(a1)
	0	1	0	0	00							0	(a1)
	1	0	0	0	00							0	(a1)
	1	1	0	0	00							0	(a1)
p	0	0	0	*p*	00							0	(a1)
	0	1	0	*p*	00							0	(a1)
	1	0	0	*p*	01							1	(a2)
	1	1	0	*p*	01							1	(a2)
q	0	0	0	*q*	00							0	(a1)
	0	1	0	*q*	01							1	(a2)
	1	0	0	*q*	00							0	(a1)
	1	1	0	*q*	01							1	(a2)
NOT *p*	0	0	0	0	00	*p*	1	01				1	(b2)
	0	1	0	0	00	*p*	1	01				1	(b2)
	1	0	0	0	00	*p*	1	11				0	(b4)
	1	1	0	0	00	*p*	1	11				0	(b4)
NOT *q*	0	0	0	0	00	*q*	1	01				1	(b2)
	0	1	0	0	00	*q*	1	11				0	(b4)
	1	0	0	0	00	*q*	1	01				1	(b2)
	1	1	0	0	00	*q*	1	11				0	(b4)
p AND *q*	0	0	0	*p*	00	*q*	0	00				0	(b1)
	0	1	0	*p*	00	*q*	0	10				0	(b3)
	1	0	0	*p*	01	*q*	0	00				0	(b5)
	1	1	0	*p*	01	*q*	0	10				1	(b7)
p NAND *q*	0	0	0	0	00	*p*	1	01	*q*	1	01	1	(c1)
	0	1	0	0	00	*p*	1	01	*q*	1	11	1	(c2)
	1	0	0	0	00	*p*	1	11	*q*	1	01	1	(c3)
	1	1	0	0	00	*p*	1	11	*q*	1	11	0	(c4)
p OR *q*	0	0	0	1	01	*p*	*q*	00				0	(b5)
	0	1	0	1	01	*p*	*q*	01				1	(b6)
	1	0	0	1	01	*p*	*q*	10				1	(b7)
	1	1	0	1	01	*p*	*q*	11				1	(b8)
p IMP *q*	0	0	0	*q*	00	*p*	1	01				1	(b2)
	0	1	0	*q*	01	*p*	1	01				1	(b6)
	1	0	0	*q*	00	*p*	1	11				0	(b4)
	1	1	0	*q*	01	*p*	1	11				1	(b8)
p NIMP *q*	0	0	0	0	00	*q*	*p*	00				0	(b1)
	0	1	0	0	00	*q*	*p*	10				0	(b3)
	1	0	0	0	00	*q*	*p*	01				1	(b2)
	1	1	0	0	00	*q*	*p*	11				0	(b4)
p RIMP *q*	0	0	0	*p*	00	*q*	1	01				1	(b2)
	0	1	0	*p*	00	*q*	1	11				0	(b4)
	1	0	0	*p*	01	*q*	1	01				1	(b6)
	1	1	0	*p*	01	*q*	1	11				1	(b8)
p RNIMP *q*	0	0	0	0	00	*p*	*q*	00				0	(b1)
	0	1	0	0	00	*p*	*q*	01				1	(b2)
	1	0	0	0	00	*p*	*q*	10				0	(b3)
	1	1	0	0	00	*p*	*q*	11				0	(b4)
p XOR *q*	0	0	0	0	00	*p*	*q*	00	*q*	*p*	00	0	(c5)
	0	1	0	0	00	*p*	*q*	01	*q*	*p*	10	1	(c6)
	1	0	0	0	00	*p*	*q*	10	*q*	*p*	01	1	(c7)
	1	1	0	0	00	*p*	*q*	11	*q*	*p*	11	0	(c4)

had already been initialized into the "0" state before W1, it would be switched into the "1" state after W1. If so, in W2 with $SV = q0$, the 00 ($q = 0$) combination would switch the Ta TE RRAM cell back into the "0" state, but the 10 ($q = 1$)

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combination could not change its state (Figure 5c), corresponding respectively to output = p AND q = 1 AND 0 = 0 (Figure 6b5) and output = p AND q = 1 AND 1 = 1 (Figure 6b7). These results have unambiguously demonstrated the feasibility of realizing 14 of 16 Boolean logic functions using the novel "one switch + one unipolar RRAM cell" hybrid structure in no more than three sequential logic cycles.

It is noteworthy that the remaining NOR and XNOR functions can be deliberately realized by performing OR and XOR functions first to get intermediate results, followed by running the NOT algorithm with previous intermediate results as input logic values. Alternatively, introducing a standard CMOS inverter in the peripheral circuit can also help to realize the NOR and XNOR functions with the "one switch + one unipolar RRAM cell" hybrid structure in no more than three sequential write cycles. For example, two sequential write cycles with SV = 00 in W1 and $SV = p(\neg q)$ in W2 can realize the NOR function, and if further followed by a third write cycle W3 with $SV = (\neg q)p$, the XNOR function can be successively realized (the "¬" herein represents the function of inverting, i.e., ¬0 = 1 and ¬1 = 0). More importantly, the present "one switch + one unipolar RRAM cell" hybrid structure provides an optimal solution for unipolar RRAM-based large-scale logic-in-memory circuits. It not only guarantees the highest integration density of $4F^2$/cell[10] but also allows the use of only one series transistor in the peripheral circuit as the switch to activate the entire system with bitwise operating philosophy (Figure S10, Supporting Information). The architecture of the computation chip can be thus significantly simplified. Meanwhile, the application scope of our logic algorithm can be further extended to phase-change RAM, which shares the identical operation mode as unipolar RRAM and promises to be a good candidate for logic-in-memory application.[49,50] Even our logic algorithm is applicable for bipolar RRAM after the correspondence between input logic values and V in Figure 5b is simply revised as "input logic 0: $V \leq V_{reset}$; input logic 1: $V \geq V_{set}$" (the bipolar RRAM here is assumed with positive V_{set} and negative V_{reset}). In future, increase in the difference between V_{set} and V_{reset} of our Ta TE RRAM cells and logic operation using pulse voltage based on nanoscale cells will be considered and conducted to further advance this work.

4. CONCLUSIONS

In summary, we propose in this work a new methodology for improving the unipolar switching uniformity by constructing cone-shape CFs with a chemically active metal cathode in unipolar metal−oxide RRAM. With the spontaneous interfacial reaction between the Ta_2O_5 switching layer and the Ta cathode, metallic Ta CFs with increased conicity are formed in the Ta/Ta_2O_5(~10 nm)/Pt unipolar RRAM cells, as visualized by high-resolution TEM observation. By restricting the rupture of cone-shaped CFs to the tip region, their residual parts will act as favorable locations for subsequent filament growth, thus suppressing the random activation of CFs and finally resulting in highly reduced switching nonuniformity with a minimum of 5.5%. Using Ta/Ta_2O_5(~10 nm)/Pt unipolar RRAM cells with improved switching uniformity, a compact "one switch + one unipolar RRAM cell" hybrid structure is experimentally demonstrated to realize all 16 Boolean logic functions for large-scale crossbar logic-in-memory circuits.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.7b19586.

Cross-sectional TEM analysis, Pt M EDS intensity profiles, variations of switching parameters with a switching cycle number, device-to-device switching uniformity analysis, comparison between the variation coefficients of switching parameters in previous works and in this work, switching endurance and retention performance, TEM observation of other CFs, O K-edge EELS analysis on CF, FFT analysis on CF, and schematic large-scale logic-in-memory circuit (PDF)

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Notes

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REFERENCES

(1) Chen, C. L. P.; Zhang, C.-Y. Data-Intensive Applications, Challenges, Techniques and Technologies: A Survey on Big Data. *Inf. Sci.* **2014**, *275*, 314−347.

(2) Borghetti, J.; Snider, G. S.; Kuekes, P. J.; Yang, J. J.; Stewart, D. R.; Williams, R. S. "Memristive" Switches Enable "Stateful" Logic Operations via Material Implication. *Nature* **2010**, *464*, 873−876.

(3) Siemon, A.; Breuer, T.; Aslam, N.; Ferch, S.; Kim, W.; van den Hurk, J.; Rana, V.; Hoffmann-Eifert, S.; Waser, R.; Menzel, S.; Linn, E. Realization of Boolean Logic Functionality Using Redox-Based Memristive Devices. *Adv. Funct. Mater.* **2015**, *25*, 6414−6423.

(4) Li, Y.; Zhou, Y.-X.; Xu, L.; Lu, K.; Wang, Z.-R.; Duan, N.; Jiang, L.; Cheng, L.; Chang, T.-C.; Chang, K.-C.; Sun, H.-J.; Xue, K.-H.; Miao, X.-S. Realization of Functional Complete Stateful Boolean Logic in Memristive Crossbar. *ACS Appl. Mater. Interfaces* **2016**, *8*, 34559−34567.

(5) Chang, Y.-F.; Zhou, F.; Fowler, B. W.; Chen, Y.-C.; Hsieh, C.-C.; Guckert, L.; Swartzlander, E. E., Jr.; Lee, J. C. Memcomputing (Memristor + Computing) in Intrinsic SiO_x-Based Resistive Switching

DOI: 10.1021/acsami.7b19586
ACS Appl. Mater. Interfaces 2018, 10, 6453−6462

Memory: Arithmetic Operations for Logic Applications. *IEEE Trans. Electron. Dev.* **2017**, *64*, 2977−2983.
(6) Waser, R.; Dittmann, R.; Staikov, G.; Szot, K. Redox-Based Resistive Switching Memories—Nanoionic Mechanisms, Prospects, and Challenges. *Adv. Mater.* **2009**, *21*, 2632−2663.
(7) Kim, K. M.; Jeong, D. S.; Hwang, C. S. Nanofilamentary Resistive Switching in Binary Oxide System: A Review on the Present Status and Outlook. *Nanotechnology* **2011**, *22*, 254002.
(8) Yang, J. J.; Strukov, D. B.; Stewart, D. R. Memristive Devices for Computing. *Nat. Nanotechnol.* **2013**, *8*, 13−24.
(9) Pan, F.; Gao, S.; Chen, C.; Song, C.; Zeng, F. Recent Progress in Resistive Random Access Memories: Materials, Switching Mechanisms, and Performance. *Mater. Sci. Eng., R* **2014**, *83*, 1−59.
(10) Seok, J. Y.; Song, S. J.; Yoon, J. H.; Yoon, K. J.; Park, T. H.; Kwon, D. E.; Lim, H.; Kim, G. H.; Jeong, D. S.; Hwang, C. S. A Review of Three-Dimensional Resistive Switching Cross-bar Array Memories from the Integration and Materials Property Points of View. *Adv. Funct. Mater.* **2014**, *24*, 5316−5339.
(11) Wong, H.-S. P.; Salahuddin, S. Memory Leads the Way to Better Computing. *Nat. Nanotechnol.* **2015**, *10*, 191−194.
(12) Chen, J.-Y.; Hsin, C.-L.; Huang, C.-W.; Chiu, C.-H.; Huang, Y.-T.; Lin, S.-J.; Wu, W.-W.; Chen, L.-J. Dynamic Evolution of Conducting Nanofilament in Resistive Switching Memories. *Nano Lett.* **2013**, *13*, 3671−3677.
(13) Chen, J.-Y.; Huang, C.-W.; Chiu, C.-H.; Huang, Y.-T.; Wu, W.-W. Switching Kinetic of VCM-Based Memristor: Evolution and Positioning of Nanofilament. *Adv. Mater.* **2015**, *27*, 5028−5033.
(14) Lee, K.; Tchoe, Y.; Yoon, H.; Baek, H.; Chung, K.; Lee, S.; Yoon, C.; Park, B. H.; Yi, G.-C. Real-Time Device-Scale Imaging of Conducting Filament Dynamics in Resistive Switching Materials. *Sci. Rep.* **2016**, *6*, 27451.
(15) Zhang, L.; Zhu, L.; Li, X.; Xu, Z.; Wang, W.; Bai, X. Resistive Switching Mechanism in the One Diode-One Resistor Memory Based on p^+-Si/n-ZnO Heterostructure Revealed by *In-Situ* TEM. *Sci. Rep.* **2017**, *7*, 45143.
(16) Gao, S.; Song, C.; Chen, C.; Zeng, F.; Pan, F. Dynamic Processes of Resistive Switching in Metallic Filament-Based Organic Memory Devices. *J. Phys. Chem. C* **2012**, *116*, 17955−17959.
(17) Wu, S.; Luo, X.; Turner, S.; Peng, H.; Lin, W.; Ding, J.; David, A.; Wang, B.; Van Tendeloo, G.; Wang, J.; Wu, T. Nonvolatile Resistive Switching in Pt/$LaAlO_3$/$SrTiO_3$ Heterostructures. *Phys. Rev. X* **2013**, *3*, 041027.
(18) Yang, Y.; Lee, J.; Lee, S.; Liu, C.-H.; Zhong, Z.; Lu, W. Oxide Resistive Memory with Functionalized Graphene as Built-in Selector Element. *Adv. Mater.* **2014**, *26*, 3693−3699.
(19) Liu, S.; Lu, N.; Zhao, X.; Xu, H.; Banerjee, W.; Lv, H.; Long, S.; Li, Q.; Liu, Q.; Liu, M. Eliminating Negative-SET Behavior by Suppressing Nanofilament Overgrowth in Cation-Based Memory. *Adv. Mater.* **2016**, *28*, 10623−10629.
(20) Liu, T.-y.; Yan, T. H.; Scheuerlein, R.; Chen, Y.; Lee, J. K.; Balakrishnan, G.; Yee, G.; Zhang, H.; Yap, A.; Ouyang, J.; Sasaki, T.; Al-Shamma, A.; Chen, C.; Gupta, M.; Hilton, G.; Kathuria, A.; Lai, V.; Matsumoto, M.; Nigam, A.; Pai, A.; Pakhale, J.; Siau, C. H.; Wu, X.; Yin, Y.; Nagel, N.; Tanaka, Y.; Higashitani, M.; Minvielle, T.; Gorla, C.; Tsukamoto, T.; Yamaguchi, T.; Okajima, M.; Okamura, T.; Takase, S.; Inoue, H.; Fasoli, L. A 130.7-mm^2 2-Layer 32-Gb ReRAM Memory Device in 24-nm Technology. *IEEE J. Solid-State Circuits* **2014**, *49*, 140−153.
(21) Sato, Y.; Tsunoda, K.; Kinoshita, K.; Noshiro, H.; Aoki, M.; Sugiyama, Y. Sub-100-μA Reset Current of Nickel Oxide Resistive Memory Through Control of Filamentary Conductance by Current Limit of MOSFET. *IEEE Trans. Electron. Dev.* **2008**, *55*, 1185−1191.
(22) Sun, X.; Li, G.; Ding, L.; Yang, N.; Zhang, W. Unipolar Memristors Enable "Stateful" Logic Operations via Material Implication. *Appl. Phys. Lett.* **2011**, *99*, 072101.
(23) Amrani, E.; Drori, A.; Kvatinsky, S. Logic Design with Unipolar Memristors *Proceedings IFIP/IEEE International Conferences on VLSI-SoC*, 2016; p 1.
(24) Jang, B. C.; Yang, S. Y.; Seong, H.; Kim, S. K.; Choi, J.; Im, S. G.; Choi, S.-Y. Zero-Static-Power Nonvolatile Logic-in-Memory Circuits for Flexible Electronics. *Nano Res.* **2017**, *10*, 2459−2470.
(25) Wald, N.; Kvatinsky, S. Design Methodology for Stateful Memristive Logic Gates *Proceedings IEEE International Conference on the Science of Electrical Engineering*, 2016; p 1.
(26) Kim, D. C.; Lee, M. J.; Ahn, S. E.; Seo, S.; Park, J. C.; Yoo, I. K.; Baek, I. G.; Kim, H. J.; Yim, E. K.; Lee, J. E.; Park, S. O.; Kim, H. S.; Chung, U.-I.; Moon, J. T.; Ryu, B. I. Improvement of Resistive Memory Switching in NiO Using IrO_2. *Appl. Phys. Lett.* **2006**, *88*, 232106.
(27) Yoon, J. H.; Kim, K. M.; Lee, M. H.; Kim, S. K.; Kim, G. H.; Song, S. J.; Seok, J. Y.; Hwang, C. S. Role of Ru Nano-Dots Embedded in TiO_2 Thin Films for Improving the Resistive Switching Behavior. *Appl. Phys. Lett.* **2010**, *97*, 232904.
(28) Uenuma, M.; Kawano, K.; Zheng, B.; Okamoto, N.; Horita, M.; Yoshii, S.; Yamashita, I.; Uraoka, Y. Resistive Random Access Memory Utilizing Ferritin Protein with Pt Nanoparticles. *Nanotechnology* **2011**, *22*, 215201.
(29) Yoon, D. H.; Kim, S. J.; Jung, J.; Lim, H. S.; Kim, H. J. Low-Voltage Driving Solution-Processed Nickel Oxide Based Unipolar Resistive Switching Memory with Ni Nanoparticles. *J. Mater. Chem.* **2012**, *22*, 17568−17572.
(30) You, B. K.; Park, W. I.; Kim, J. M.; Park, K.-I.; Seo, H. K.; Lee, J. Y.; Jung, Y. S.; Lee, K. J. Reliable Control of Filament Formation in Resistive Memories by Self-Assembled Nanoinsulators Derived from a Block Copolymer. *ACS Nano* **2014**, *8*, 9492−9502.
(31) Shin, K.-Y.; Kim, Y.; Antolinez, F. V.; Ha, J. S.; Lee, S.-S.; Park, J. H. Controllable Formation of Nanofilaments in Resistive Memories via Tip-Enhanced Electric Fields. *Adv. Electron. Mater.* **2016**, *2*, 1600233.
(32) Kwon, D.-H.; Kim, K. M.; Jang, J. H.; Jeon, J. M.; Lee, M. H.; Kim, G. H.; Li, X.-S.; Park, G.-S.; Lee, B.; Han, S.; Kim, M.; Hwang, C. S. Atomic Structure of Conducting Nanofilaments in TiO_2 Resistive Switching Memory. *Nat. Nanotechnol.* **2010**, *5*, 148−153.
(33) Kurnia, F.; Liu, C.; Jung, C. U.; Lee, B. W. The Evolution of Conducting Filaments in Forming-Free Resistive Switching Pt/TaO_x/Pt Structures. *Appl. Phys. Lett.* **2013**, *102*, 152902.
(34) Prakash, A.; Jana, D.; Maikap, S. TaO_x-based Resistive Switching Memories: Prospective and Challenges. *Nanoscale Res. Lett.* **2013**, *8*, 418.
(35) Gao, S.; Zeng, F.; Wang, M.; Wang, G.; Song, C.; Pan, F. Tuning the Switching Behavior of Binary Oxide-Based Resistive Memory Devices by Inserting an Ultra-Thin Chemically Active Metal Nanolayer: A Case Study on the Ta_2O_5−Ta System. *Phys. Chem. Chem. Phys.* **2015**, *17*, 12849−12856.
(36) Kim, K. M.; Choi, B. J.; Shin, Y. C.; Choi, S.; Hwang, C. S. Anode-Interface Localized Filamentary Mechanism in Resistive Switching of TiO_2 Thin Films. *Appl. Phys. Lett.* **2007**, *91*, 012907.
(37) Kim, K. M.; Park, T. H.; Hwang, C. S. Dual Conical Conducting Filament Model in Resistance Switching TiO_2 Thin Films. *Sci. Rep.* **2015**, *5*, 7844.
(38) Chang, S. H.; Chae, S. C.; Lee, S. B.; Liu, C.; Noh, T. W.; Lee, J. S.; Kahng, B.; Jang, J. H.; Kim, M. Y.; Kim, D.-W.; Jung, C. U. Effects of Heat Dissipation on Unipolar Resistance Switching in Pt/NiO/Pt Capacitors. *Appl. Phys. Lett.* **2008**, *92*, 183507.
(39) Miao, F.; Strachan, J. P.; Yang, J. J.; Zhang, M.-X.; Goldfarb, I.; Torrezan, A. C.; Eschbach, P.; Kelley, R. D.; Medeiros-Ribeiro, G.; Williams, R. S. Anatomy of a Nanoscale Conduction Channel Reveals the Mechanism of a High-Performance Memristor. *Adv. Mater.* **2011**, *23*, 5633−5640.
(40) Lee, J.; Du, C.; Sun, K.; Kioupakis, E.; Lu, W. D. Tuning Ionic Transport in Memristive Devices by Graphene with Engineered Nanopores. *ACS Nano* **2016**, *10*, 3571−3579.
(41) Li, X. Y.; Shao, X. L.; Wang, Y. C.; Jiang, H.; Hwang, C. S.; Zhao, J. S. Thin TiO_x Layer as a Voltage Divider Layer Located at the Quasi-Ohmic Junction in the Pt/Ta_2O_5/Ta Resistance Switching Memory. *Nanoscale* **2017**, *9*, 2358−2368.

DOI: 10.1021/acsami.7b19586
ACS Appl. Mater. Interfaces 2018, 10, 6453−6462

(42) Wang, S.-Y.; Lee, D.-Y.; Tseng, T.-Y.; Lin, C.-Y. Effects of Ti Top Electrode Thickness on the Resistive Switching Behaviors of RF-Sputtered ZrO_2 Memory Films. *Appl. Phys. Lett.* **2009**, *95*, 112904.
(43) Kim, K. M.; Hwang, C. S. The Conical Shape Filament Growth Model in Unipolar Resistance Switching of TiO_2 Thin Film. *Appl. Phys. Lett.* **2009**, *94*, 122109.
(44) Menzel, S.; Adler, N.; van den Hurk, J.; Tappertzhofen, S.; Valov, I.; Waser, R. Simulation of Polarity Independent RESET in Electrochemical Metallization Memory Cells *5th IEEE International Memory Workshop*, 2013; p 92.
(45) Wang, M.; Zhou, J.; Yang, Y.; Gaba, S.; Liu, M.; Lu, W. D. Conduction mechanism of a TaO_x-based selector and its application in crossbar memory arrays. *Nanoscale* **2015**, *7*, 4964−4970.
(46) Schindler, C.; Staikov, G.; Waser, R. Electrode kinetics of Cu−SiO_2-based resistive switching cells: Overcoming the voltage-time dilemma of electrochemical metallization memories. *Appl. Phys. Lett.* **2009**, *94*, 072109.
(47) Cooper, D.; Baeumer, C.; Bernier, N.; Marchewka, A.; La Torre, C.; Dunin-Borkowski, R. E.; Menzel, S.; Waser, R.; Dittmann, R. Anomalous Resistance Hysteresis in Oxide ReRAM: Oxygen Evolution and Reincorporation Revealed by In Situ TEM. *Adv. Mater.* **2017**, *29*, 1700212.
(48) Park, G.-S.; Kim, Y. B.; Park, S. Y.; Li, X. S.; Heo, S.; Lee, M.-J.; Chang, M.; Kwon, J. H.; Kim, M.; Chung, U.-I.; Dittmann, R.; Waser, R.; Kim, K. *In Situ* Observation of Filamentary Conducting Channels in an Asymmetric Ta_2O_{5-x}/TaO_{2-x} Bilayer Structure. *Nat. Commun.* **2013**, *4*, 2382.
(49) Cassinerio, M.; Ciocchini, N.; Ielmini, D. Logic Computation in Phase Change Materials by Threshold and Memory Switching. *Adv. Mater.* **2013**, *25*, 5975−5980.
(50) Wong, H.-S. P.; Raoux, S.; Kim, S.; Liang, J.; Reifenberg, J. P.; Rajendran, B.; Asheghi, M.; Goodson, K. E. Phase Change Memory. *Proc. IEEE* **2010**, *98*, 2201−2227.

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