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ARTICLE

Light-Gated Memristor with Integrated Logic and Memory Functions

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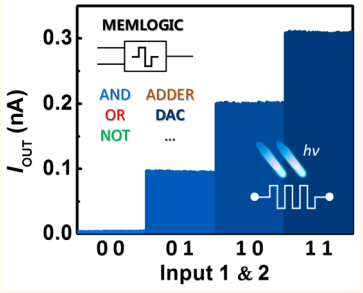
Supporting Information

ABSTRACT: **Memristive devices are able to store and process information, which offers several key advantages over the transistor-based architectures. However, most of the two-terminal memristive devices have fixed functions once made and cannot be reconfigured for other situations. Here, we propose and demonstrate a memristive device "*memlogic*" (memory logic) as a nonvolatile switch of logic operations integrated with memory function in a single light-gated memristor. Based on nonvolatile light-modulated memristive switching behavior, a single memlogic cell is able to achieve optical and electrical mixed basic Boolean logic of reconfigurable "AND", "OR", and "NOT" operations. Furthermore, the single memlogic cell is also capable of functioning as an optical adder and digital-to-analog converter. All the memlogic outputs are memristive for *in situ* data storage due to the nonvolatile resistive switching and persistent photoconductivity effects. Thus, as a memdevice, the memlogic has potential for not only simplifying the programmable logic circuits but also building memristive multifunctional optoelectronics.**



KEYWORDS: *memristive switching, persistent photoconductance, light-gated memristor, memlogic, memcomputing*

Programmable logic circuits that are dynamically reconfigurable for the running of different algorithms have been considered as an effective approach to enhance the computing performance in the post-Moore era.[1−5] Compared to the current hardware-determined logic processor with only one designed function, the high reprogram ability of these circuits makes them more efficient in dealing with application-specific tasks like machine learning and data analytics. Promising candidates include a complex programmable logic device (CPLD), field-programmable gate array (FPGA), *etc.* However, state-of-the-art programmable logic devices lie in the complex programmable routing matrix that connects the logic blocks with unpredictable signal transmission delay and large bulky volume. The volatile nature of the logic gate arrays also requires additional random access memory (RAM) block to store the assigned function and output data.[6−8] Although the reconfigurable logic gates have been made with memristive devices[9] such as magnetoresistance element and memristor recently,[2−4] they still need additional magnetic field or polarized current as inputs and have to involve multiple-step algorithms and operations.

Here, we propose and demonstrate a memdevice—*memlogic* (memory logic), which is a nonvolatile hardware-reconfigurable logic gate based on a single light-gated memristor (Figure 1a). In order to achieve the memlogic, resistive switching and persistent photoconductivity effects are combined in a nonvolatile light-gated memristor through reversible tuning the interfacial barrier profile with voltage and light stimuli in the ITO/CeO_{2-x}/AlO_y/Al multilayer structure. Using light and voltage as logic or configuring inputs and the resistance states as output, the single light-gated memristor is capable of functioning as a nonvolatile and reconfigurable logic gate including "AND", "OR", and "NOT" operations, as well as optical adder and digital-to-analog converter (DAC). Moreover, both the endued logic functions and output signals can be stored *in situ* in the same device through the nonvolatile optoelectronic resistance switching behavior for eliminating the von Neumann bottleneck. Thus, we name the present optoelectronic device as memlogic, which is short for memory logic with both nonvolatile configuration of logic functions and nonvolatile logic output results. Using a 5 by 5 memlogic array, we demonstrated a proof-of-concept image processor. As a

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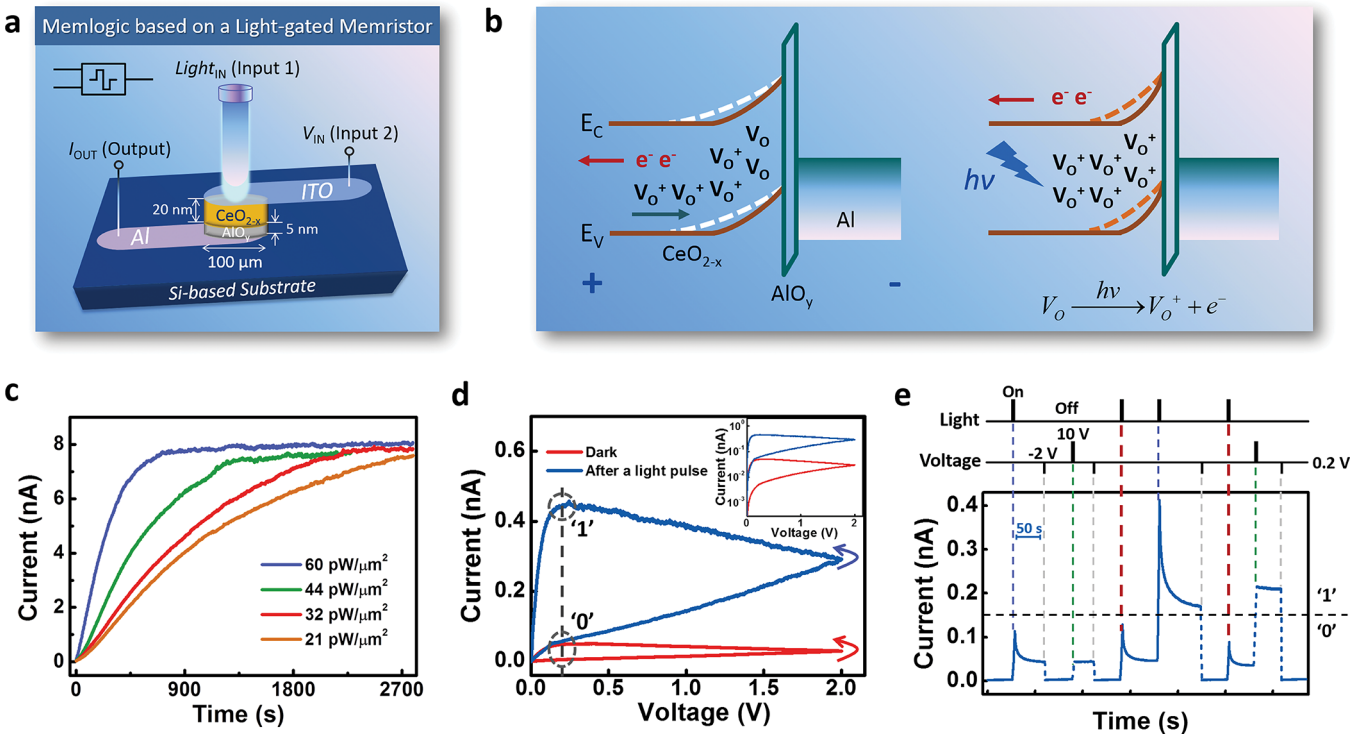

Figure 1. Schematic illustration of the structure, working mechanism and basic optoelectronic properties of the memlogic device. (a) Schematic diagram of the optoelectronic memlogic with ITO/CeO_{2-x}/AlO_y/Al structure. (b) Mechanism for the light-gate memristive characteristics of the device. Schematic energy band diagram with different operations: (left) electrically writing, (right) optical gating. The red arrows indicate the direction of electron migration, and the gray arrow indicates the direction of V_O^+ migration. (c) Current increasing with illumination time increasing under different light intensities −21, 32, 44, and 60 pW/μm^2. The read voltage is 0.2 V. (d) Memristive switching of the device before and after light gating at the positive voltage sweep. The inset shows the log-scale *I*−*V* curve. (e) Optical and electrical hybrid-mode-controlled resistance switching. The read voltage is 0.2 V.

memristive device, the optoelectronic memlogic may have high potential for not only building memristive multifunctional optoelectronic devices[10−12] but also simplifying the programmable logic circuits, in-memory computing, and artificial intelligence.[13−23]

RESULTS AND DISCUSSION

Generally, two variables are required as the inputs to manipulate the resistance output signals of a device for the implementation of Boolean logic functions.[24] In order to realize Boolean logic functions in a single device, our strategy is to use both electrical and optical means to control the resistance states *via* modulating the interfacial charge trapping and detrapping[12] of an ITO/CeO_{2-x}/AlO_y/Al structured device (as shown in Figures 1a and S1). Herein, cerium oxide thin film has been chosen as the functioning layer because it is resistance switchable and photosensitive in the broadband from UV to visible due to the defect energy levels in the band gap.[25,26] Moreover, due to the difference of the Fermi level from the Al layer surface, the cerium oxide thin film will form a Schottky barrier with the native AlO_y/Al layer.[26] When the ITO electrode is positively biased, the electrons trapped in the oxygen vacancies of the interfacial space charge region will be released and driven to ITO electrode, and the oxygen vacancies with positive charge will be driven to the interface. These processes generate additional positively charged oxygen vacancies (V_O^+) in the interfacial region and then lower the effective interfacial barrier (Figure 1b, left). With the introduction of light stimuli onto the resistance switchable ITO/CeO_{2-x}/AlO_y/Al structure (Al electrode grounded and ITO electrode biased), electrons trapped within the interfacial CeO_{2-x} layer adjacent to the AlO_y intercalation can be further excited by photons, leaving more positively charged oxygen vacancies at the interface. This will facilitate the narrowing of the effective Schottky barrier of the CeO_{2-x}/AlO_y/Al region and decrease the device resistance persistently (Figure 1b, right). In this process, the wavelength window of photoresponse was broadened to the visible region due to the oxygen defect level in the band gap.[26] To erase the nonvolatile light-modulated barrier profile and resistance states, a negative bias on the ITO electrode is needed to recover the barrier profile to its initial state by the negative charge injection to the interfacial space charge region. Thus, the electrical resistive switching behaviors of the multilayer device will be further modulated by light due to the persistent photoconductance effect, which constitute the feature of the light-gated memristor-based memlogic.

The experimental resistive switching behavior of the ITO/CeO_{2-x}/AlO_y/Al structure is shown in Figure S2. A positive voltage sweeping from 0 to 2 V toggles the device from the initial resistance state to a lower resistance state due to the V_O^+ accumulating at the interface with an ON/OFF ratio of ∼14 (read at 0.2 V), while a negative voltage sweeping from 0 to −2 V performs the opposite operation. The obvious rectification effect with a rectifying ratio of ∼4800 (read at ±2 V) directly confirms the existence of a Schottky barrier at the defective n-type cerium oxide/AlO_y/Al interfacial region shown in Figure 1a,b. All the optoelectronic functions realized in this study are

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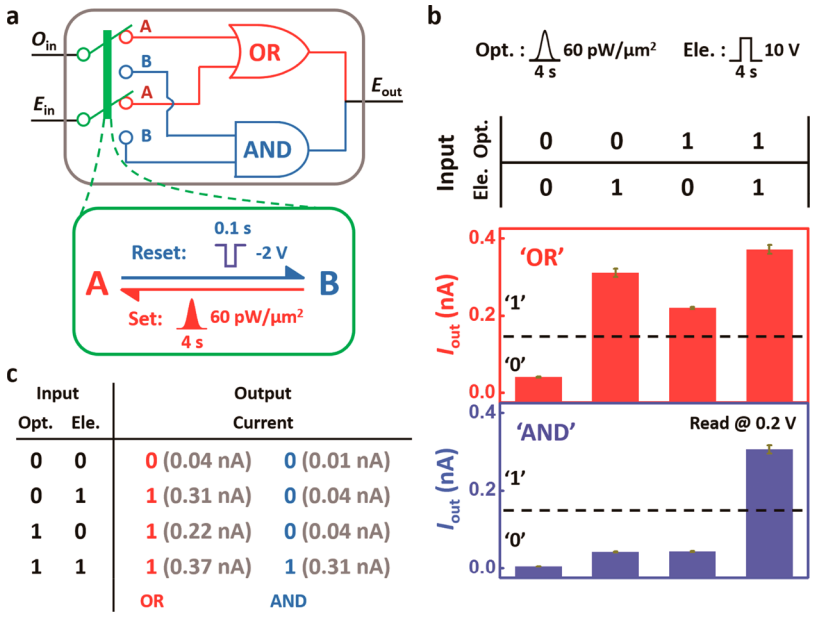

Figure 2. Memlogic operation of reconfigurable "AND" and "OR" gates. (a) Schematic diagram of the "AND" and "OR" logic operation switching. "Optical-set" process: transition from "AND" gate to "OR" gate stimulated with a light pulse. "Electrical-reset" process: transition from "OR" gate to "AND" gate by a negative voltage pulse. (b) Reprogrammable electrical outputs of the memlogic with a pair of optical (Opt.) and electrical (Ele.) inputs. (c) Truth table and output current values of the memlogic "AND" and "OR". Read at 0.2 V.

based on manipulating the profile of this Schottky barrier. After repeatedly illuminating the device with visible emission of a halogen lamp at 60 pW/μm^2 for 4 s, accumulated and persistent photocurrents are observed due to the photogenerated V_O^+ at the interface (Figures 1c and S3). When the interfacial Schottky barrier width is restored by reinjection of electrons or oxygen ions into the space region with a voltage pulse of −2 V and 0.1 s, the photoresponse can be reversibly erased, therefore completing the "optical-set/electrical-reset" operation cycle of the optoelectronic memristor device (Figure S3). To better understand the mechanism of the optical-set process, various light stimulations with different light intensities were used to study the dynamic optical modulation of device resistance states (Figure 1c). When increasing the illumination time, the current first increased and then reached a stable level due to more and more photoinduced oxygen vacancies generated to a saturated concentration at the interface, which will lower the effective barrier and interfacial resistance to a saturated level. With the increasing of light intensity from 21 pW/μm^2 to 32, 44, and 60 pW/μm^2, the photocurrents increase faster and need shorter time to reach to the identical saturated level at about 8 nA, and the conducting behavior of the metal−insulator−semiconductor (MIS) interface becomes Ohmic conducting behavior from Schottky barrier-induced rectification conducting behavior by the photoinduced doping at the interface (Figure S4). This photoinduced doping is different from conventional photoconductivity effect, wherein the photogenerated charges cannot affect the contact barrier at the MIS interface. In the ITO/CeO_{2-x}/AlO_y/Al structured device, the photoinduced doping of positively charged oxygen vacancies (V_O^+) at the CeO_{2-x}/AlO_y/Al interface will narrow the width of the barrier and decrease the nonvolatile resistance states. In addition, the quantity of V_O^+ needed to reach to the same saturated photocurrent level is identical under different light illuminations. Therefore, the light with higher intensity will need shorter time to stimulate the device to the same saturated current level and have higher switching speed, as shown in Figure 1c. Additionally, based on the illumination time-dependent states, multilevel memory also can be achieved by modulating the light pulse width in the optical-set process.

The photosensitive nature of the ceria media[25,26] also modulates the electrically resistive switching behavior of the memristor devices (Figure 1d). The currents of both bistable states are further increased to higher levels (blue curve) from their initial $I-V$ loop (red curve) by the optical gating effect with a light pulse of 60 pW/μm^2 amplitude and 4 s duration. Additionally, the negative differential resistance (NDR) effect exists in back DC sweep from 2 to 0 V both before and after being subjected to light irradiation. According to the mechanism shown in Figure 1b, if a positive voltage was applied on the ITO electrode and a negative voltage on the Al electrode, the electrons trapped in the interfacial oxygen vacancies will be released and driven to the ITO electrode, whereas the oxygen vacancies with positive charge will be driven to the interface. These processes generate additional positively charged oxygen vacancies (V_O^+) in the interfacial region and then lower the effective interfacial barrier, which is the key factor to increase the current. So, in both the forward and backward sweeping between 0 and 2 V, as long as the voltage is positive and high enough to release the trapped electrons, the current will increase. Therefore, the $I-V$ curve of the back positive DC sweep from 2 to 0 V shows NDR effect. Considering the significant difference between the current level in the lowest resistance state (LRS) and those in the other three states including two higher resistance states (HRS) and one initial resistance state (IRS), logical 1 and 0 can be directly defined with the current levels above and below 150 pA (read at 0.2 V), respectively. Thus, a nonvolatile logic switch with mixed optical and electrical inputs can be achieved with a single cell of the present light-gated memristor. The optical and electrical hybrid control of the resistive switching behavior is also estimated in the pulse mode of Figure 1e. Being consistent with the results shown in Figure 1d, a single optical (60 pW/μm^2 amplitude and 4 s duration) or voltage (10 V amplitude

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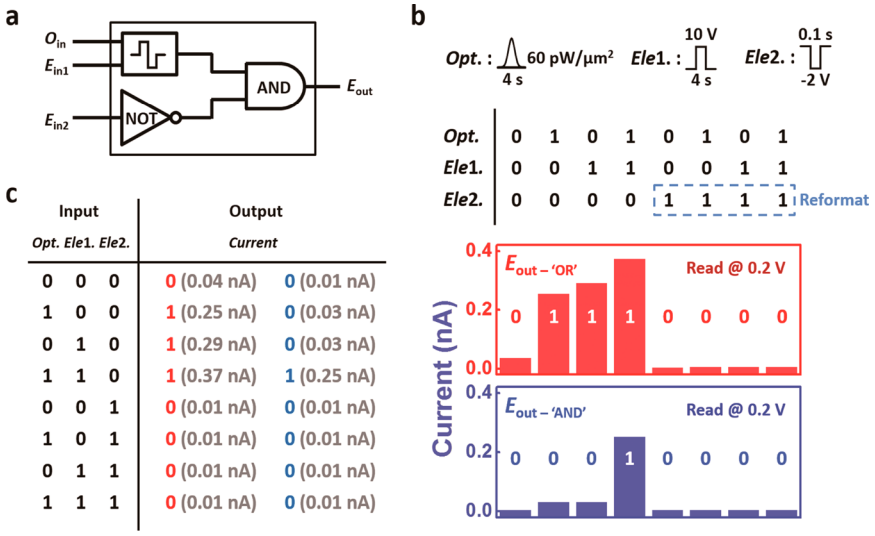

Figure 3. Reformatting of the memlogic device through "NOT" operation. (a) Complicated memlogic gate introducing "NOT" operation that reformats the memlogic gate to a blank device. E_{in2} is the second electrical input to reformat the device. (b) Complicated memlogic operation and (c) respective truth table of the memlogic gate with an additional electrical input (E_{in2}). The bars in red represent the output logic gate with the memlogic in "OR" operation state, and the blue represents the output logic gate with the memlogic in "AND" operation state.

and 4 s duration) pulse is capable of switching the device from IRS (~4 pA) to HRS (~40 pA), whereas the LRS (above 150 pA) or logical 1 is obtained only when two sets of the optical pulses or both the optical and electrical pulses are present. Herein, the first set of light pulses (marked by red dash line) is defined as an "optical-set" operation, upon which the superimposition of the subsequent electrical or optical pulse will switch the device to the LRS state. Again, a negative voltage pulse of −2 V/0.1 s is sufficient to reset all states to IRS, which enables the devices to be rewritable. These optoelectronic properties of the nonvolatile and reversible light-gated memristor shown in Figure 1 constitute the basic memlogic operations discussed later. On the basis of previously reported photoresponsive memristors,[27−33] the proposed interfacial Schottky junction-based memristor allows simultaneously nonvolatile, accumulative, and electrically reversible light modulation of memristive behavior due to reversible control of the interfacial barrier. Therefore, besides the possible applications of photodetector-in-memory, multilevel optoelectronic memory, we exploit and design a memdevice—memlogic (memory logic)—and demonstrate the possible applications of the proof-of-concept memlogic for nonvolatile hardware-reconfigurable logic-in-memory devices.

In the current state-of-the-art programmable logic circuits, FPGA or CPLD for instance, the complex routing matrix that connects the fixed-functioning logic blocks in a particularly programmed manner determines the overall functionality of the chip. As the logic function of each individual building component is hardware-determined as factory settings, the field-programmable characteristics highly depend on the reconstruction of the complex routing matrix and are thus practically less efficient. As such, the reconfigurability of logic devices is possibly a determining factor that helps to simplify the architecture of the programmable logic circuits and enhance their performance. In the proposed memlogic device, a pair of the applied voltage and light pulses form two independent inputs (O_{in} and E_{in}) of the optoelectronic device to control the output resistance signals (E_{out}). Figure 2a shows the schematic operation principle of a typical memlogic cell. The initial logic function of the device is "AND". When stimulated by a light pulse in the optical-set process, the memlogic cell switches to an "OR" gate, with the logical 0 (below 150 nA) obtained only when both the optical and electrical inputs (top panel of Figure 2b) are absent. Logical 1 (above 150 nA) will be obtained otherwise (middle panel of Figure 2b). This behavior is consistent with the results plotted in Figure 1e. With an electrical-reset process, the "OR" gate is reconfigured to the initial "AND" gate. Only when both the optical and electrical inputs are present, the logical 1 (above 150 nA) will be obtained; otherwise, the output will be logical 0 (below 150 nA in the bottom panel of Figure 2b). The truth table of the memlogic, as shown in Figure 2c, has two columns of output values, which are consistent with the bistable logic operations of the "OR" and "AND" gate, respectively. Therefore, the optical-set/electrical-reset operations allow the present device to be a reconfigurable logic element that may be used to switch between different algorithms to efficiently reduce the circuit complexity and increase the effective integrating density of the processor chip.

"NOT" operation is the other basic function to complete a logic block. Besides the optical-set/electrical-reset operations that reconfigure the device between "OR" and "AND" gates, an electrical reformatting process that can serve as the "NOT" operation to erase the endued program and output signals is essential for releasing the memlogic cell for subsequent workloads.[10] Herein, a voltage pulse of −2 V/0.1 s is used as the second electrical input E_{in2} (Figure 3a), and the final output depends on both the three input signals and the present logic operation state of the memlogic cell. Without the introduction of E_{in2}, the output of the memlogic depends on the input signals and corresponds to the preloaded logic operation state of the "OR" or "AND" gate. When E_{in2} is applied, the device currents are all erased to about 4 pA and the output of the memlogic is always logical 0 (below 150 nA), regardless of the previous logic operation state and inputs. Thus, the memlogic device is reformatted in this "NOT" operation to a blank cell for any further operations with the reconfigurable choices of "AND" and "OR". Therefore, a complex logic gate with three

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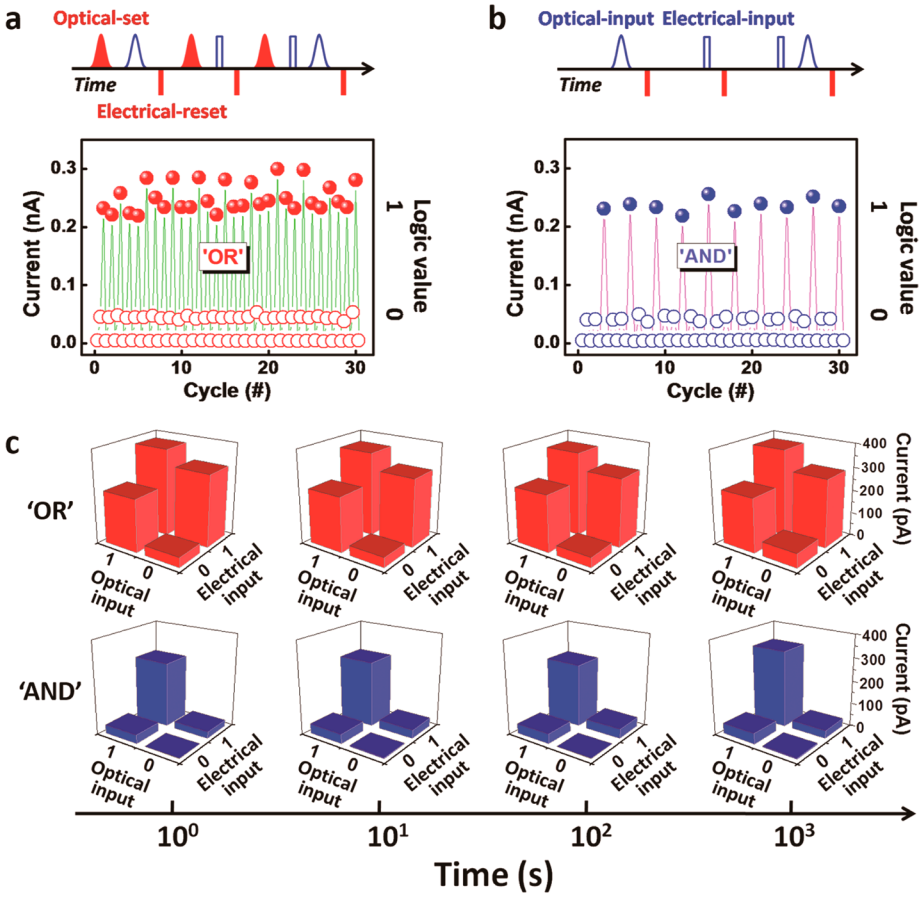

Figure 4. Cyclic reconfiguring and logic operating of the (a) "OR" and (b) "AND" gates. The red spheres demonstrate the "OR" gate switching between logical 0 (hollow spheres) and logical 1 (solid spheres), whereas the blue spheres demonstrate the "AND" gate switching between logical 0 (hollow spheres) and logical 1 (solid spheres). Memory characteristics of the (c) endued logic operation of the memlogic. The read voltage is 0.2 V.

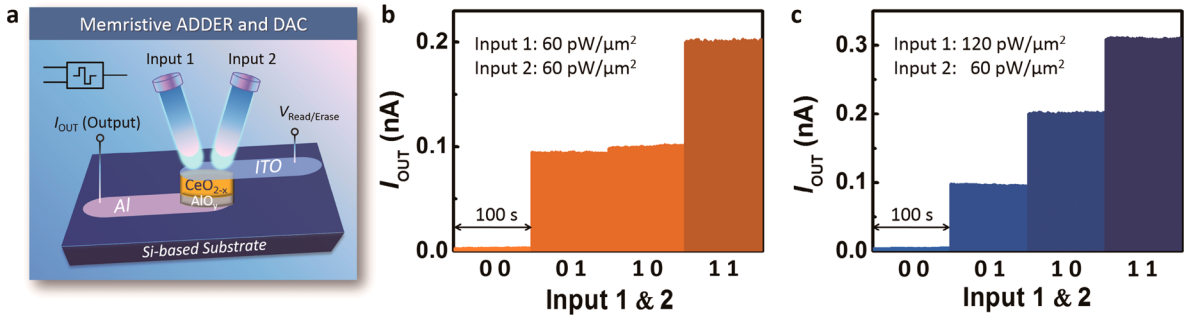

Figure 5. Memristive ADDER and digital-to-analog converter. (a) Schematic diagram of two-bit memristive ADDER and DAC with a single memlogic cell. Light/dark of each independent optical input corresponds to digital 1/0. (b) With identical intensity (60 pW/μm^2) of the two input light beams, the memlogic is operating as an optical ADDER element, which adds two digital optical input signals and output an analog equivalent of the digital sum. (c) With specific light intensity (120 pW/μm^2 for input 1 and 60 pW/μm^2 for input 2), the memlogic is operating as an optical DAC element, in which the analog current output corresponds to digital inputs from 00 to 11.

input signals is also demonstrated. The respective optoelectronic responses and truth table are shown in Figure 3b,c. It is also noteworthy that in order to perform the "NOT" operation, the erasing input E_{in2} must be loaded after the other two. By monitoring the magnitude of the output signal, the sequence of loading O_{in}/E_{in1} and E_{in2} can easily discriminated, therefore implementing additional timing generator function to the present memlogic cells and making it more powerful.

The reconfigurability of the memlogic devices shows promising endurance characteristics for both the "set-logic-read-format" process of the "OR" gate and "reset-logic-read-format" process of the "AND" gate (Figure 4a,b). In each cycle of reconfiguration, the output currents are about 40 pA after being set to the "OR" gate with an optical pulse stimulus or 4 pA after being reset to the "AND" gate with an electrical pulse stimulus, either of which represents the logical 0 (below 150 nA). When the optical and electrical input pairs of "01" or "10" are loaded, the memlogic outputs are logical 0 for the "AND" gate and logical 1 for the "OR" gate. With the logical inputs of "11", the output of the memlogic is logical 1 for both gates.

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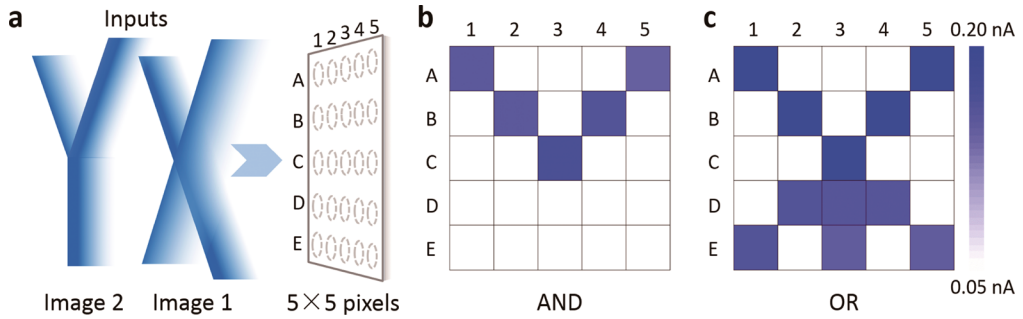

Figure 6. Proof-of-concept demonstration of image recognizing and memorizing. (a) Images of "X" and "Y" were input into a 5 by 5 memlogic array when all the memlogic cells were reset to HRS (b) or LRS (c). In (b), the output current image is the result of logic output of images "X" and "Y". In this case, the memlogic array is capable of recognizing the same part in different images and acting as SAME FINDER. In (c), the output current image is the result of logic output of images "X" or "Y". Then, the memlogic array is able to recognize the part in either image and act as ALL FINDER.

When the logic manipulation is done, a reformatting process can be applied to make the memlogic device fresh. With their respective optical and electrical inputs, the output currents of the two corresponding logic gates can remain with promising accuracy after tens of the "set-logic-read-format" and "reset-logic-read-format" cycles, thus making the memlogic devices reconfigurable and reprogrammable (Figure 4a,b). More importantly, due to the nonvolatile nature of the electrical memristive switching behavior and the persistent characteristics of the photoconductance effect, all the eight current levels corresponding to the two logic operations remain stable in air, which allows the nonvolatile storage of both the logic functions and the logic outputs (Figure 4c). As such, the possibility of attaching memory capability to the logic unit may eliminate the additional RAM blocks in the traditional programmable logic circuits and also will help to solve the data transmission bottleneck problem in the current state-of-the-art von Neumann architecture computer systems.[16−19]

Furthermore, using two light beams as inputs to control states, the single memlogic cell is also capable of performing as memristive optical ADDER and DAC due to the linear relationship between stateful current and light intensity (Figure 5a).[26] Herein, when the two input light pulses are at the identical intensity of 60 pW/μm^2 and duration of 10 s, the memlogic is an adder. Figure 5b shows a two-bit, digital optical input, current states analog output ADDER element, wherein the memlogic adds two digital optical input signals and output an analog equivalent of the digital sum. Additionally, these results also serve as an optoelectronic OR gate under appropriate logic conditions. The adding operation can be extended to design multibit, digital optical input by introducing more optical illumination in the single memlogic cell. Figure 5c presents a two-bit optoelectronic DAC. To achieve the DAC function in a single memlogic cell, the two optical inputs are at specific intensity (120 pW/μm^2 for input 1 and 60 pW/μm^2 for input 2). The two independent optical inputs could be light or dark, which correspond to digital binary inputs 00, 01, 10, and 11. The corresponding output is the analog equivalent of these inputs. Moreover, all the outputs of the above two operations are also nonvolatile and can be stored *in situ*. Therefore, the proof-of-concept memlogic is also capable of performing as nonvolatile ADDER and DAC, which will extend the memlogic applications to more complex optoelectronic logic-in-memory devices.

Based on digital optical information processing function in a single memlogic cell, a memlogic array is able to realize image processing. Figure 6 shows the proof-of-concept demonstration of image recognizing and memorizing with a 5 by 5 memlogic array. Two images of "X" and "Y" shapes of visible light (600 nm) are with 4 s duration pulses as inputs and current map as output, when all the memlogic cells were reset to HRS; the currents of the memlogic cells were illuminated once at about 0.04 nA (lower than 0.05 nA as logical 0), and the currents of the memlogic cells were illuminated twice at about 0.15 nA (logical 1 shown in Figure S5a). So the array is able to find the twice-illuminated memlogic cells at the same part in both "X" and "Y" images. It is the nonvolatile "V" shape output current map shown in Figure 6b. Therefore, the memlogic array is able to recognize and memorize the same part in different images, and we name it SAME FINDER. Furthermore, due to the reconfigurability of memlogic, when all the memlogic cells were set to LRS, the currents of the memlogic cells were illuminated at least once at about 0.15 nA, as shown in Figure S5b. Therefore, the array is able to find the at least once-illuminated memlogic cells in either part in "X" or "Y" images (Figure 6c), thus allowing the memlogic array to recognize and memorize either part in different images, and we name it ALL FINDER. Therefore, SAME and ALL FINDERs can be realized in the same memlogic array.

To further exploit the potential of memlogic, the performance of memlogic should be improved. For instance, the speed of memlogic in this stage is low and insufficient for logic circuits. However, the speed will be accelerated by increasing light intensity or using more sensitive short-wave band light as input. Under the light illumination with higher intensity or shorter wavelength, the photocurrent increases faster, which can be predicted by the relationship of dynamic photocurrent increasing with time under light illumination with different intensities (Figure 1c) or wavelengths.[26] Higher built-in electric field will also accelerate the separation of trapped electrons and trapping sites (oxygen vacancies) and consequently shorten the device response time. Here, the built-in electric field depends on both the work function difference between that of metal electrodes and semiconductor medium layer and the width of the space charge region. The larger the difference of work functions and the narrower the space charge region, the higher the built-in electric field will be. The width of the space charge region can be narrowed by increasing the defect concentration. So, using electrode metals with higher work function or introducing more oxygen vacancy defects at the interface may increase the built-in electric field and then lead to shorter response time. Additionally, for the scaling aspect, the light

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source and light spot are relatively large in this work, which limits the scaling of the memlogic device. Nevertheless, with the rapid development of nanophotonics, the diameter of light spot has been reduced to nanoscale,[34] which is comparable to the nanoscale of the memristor and may lead to a high density memlogic device for nanoimage processing.

CONCLUSIONS

To summarize, by combining the memristive switching and persistent photoconductivity effects in the ITO/CeO_{2-x}/AlO_y/Al structure, a conceptual memlogic device is proposed and demonstrated. The as-proposed proof-of-concept memlogic offers several key advantages over the conventional transistor-based logic devices: (i) It is simple. A single memlogic cell, rather than a bundle of transistors, is capable of performing certain logic operations with optical and electrical hybrid methods. (ii) It is reconfigurable. A single memlogic cell is capable of functioning as logic AND, OR, NOT, and ADDER, DAC. A memlogic array is also capable of functioning as a reprogrammable image processor. Compared with the CMOS logic gates in CPLD or FPGA, this memlogic with self-reconfiguration may be a fundamental improvement to simplify the complex programmable routing matrix.[2,22] (iii) It is nonvolatile. The *in situ* storage of the endued logic functions and outputs in the same device can help to eliminate the RAM blocks in FPGA and avoid von Neumann bottleneck in modern computing systems.[16,35−45] All of these features are beneficial for lowering the complexity of the circuit architecture and enhancing the computation performance. Furthermore, a simple memlogic with reconfigurable logic and *in situ* memory is comparable with the functions of neurons, which process and store information parallel in the same unit. An optoelectronic network with the memlogic devices could perform massively parallel data communicating and reprogrammable nonvolatile computing, which might provide a possible way to design a brain-like optoelectronic artificial intelligence network. Therefore, as a memdevice, the optoelectronic memlogic may have high potential for reconfigurable logic-in-memory computing, integrated photonics, and artificial intelligence.

METHODS

Device Fabrication and Measurement. A 30 nm thick aluminum electrode was first deposited by electron-beam evaporation on a commercial Si-based substrate. The polycrystalline CeO_{2-x} layer with the thickness of about 20 nm (Figure S1) was deposited by a magnetron-sputtering technique. Finally, the 100 μm diameter conductive and transparent ITO electrodes with the thickness of about 100 nm were deposited by pulsed laser deposition. The device structure including cross section image and elements distribution (energy-dispersive spectroscopy, EDS mapping) was characterized by a JEOL 2100F transmission electron microscope in SAE Magnetics (H.K.) Ltd. Company. The basic characterization and measurements, including XRD pattern, UV−visible absorption spectrum, X-ray and ultraviolet photoelectron spectroscopic (SHIMADZU, AXIS ULTRA DLD) measurements were shown in the Supporting Information of ref 26.

Optoelectronic Characterization. The visible light pulses were generated by the halogen lamp. The intensities of the light pulses used in this work were calibrated by a Li-250A light meter (LI-COR, Inc.). The electrical current−voltage (I−V) characteristics of the ITO/CeO_{2-x}/AlO_y/Al structured devices were measured with the precision semiconductor parameter analyzer (Keithley 4200) attached to a Lakeshore probe station with a dark chamber, in which all the optoelectronic measurements will not be influenced by the environment lights.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.7b05762.

More detailed information about the cross section TEM image of the device structure, resistive switching behavior, persistent photoconductivity, I−V curve fitting, and current change of an individual memlogic cell with different position under image inputs (PDF)

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